

8

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,Folsten_MBP17

06/15/09

Page

Contents

Sync

1

Table of Contents

K20_MLB

2

System Block Diagram

M98_MLB

3

Power Block Diagram

RXU_K20

4

Revision History

NA

5

BOM Configuration

K20A_MLB

6

JTAG Scan Chain

BEN_K20

7

Functional / ICT Test

K20_MLB

8

Power Aliases

RXU_K20

9

Signal Aliases

K20_MLB

10

CPU FSB

M98_MLB

11

CPU Power & Ground

M98_MLB

12

CPU Decoupling & VID

M98_MLB

13

extended Debug Port(MiniXDP)

M98_MLB

14

MCP CPU Interface

T18_MLB

15

MCP Memory Interface

T18_MLB

16

MCP Memory Misc

T18_MLB

17

MCP PCIe Interfaces

T18_MLB

18

MCP Ethernet & Graphics

T18_MLB

19

MCP PCI & LPC

T18_MLB

20

MCP SATA & USB

T18_MLB

21

MCP HDA & MISC

T18_MLB

22

MCP Power & Ground

T18_MLB

23

MCP Standard Decoupling

M98_MLB

24

MCP Graphics Support

M98_MLB

25

SB Misc

M98_MLB

26

FSB/DDR3/FRAMBUF Vref Margining

BEN_K20

27

DDR3 SO-DIMM Connector A

BEN_K20

28

DDR3 SO-DIMM Connector B

BEN_K20

29

DDR3 Support

M98_MLB

30

Right Clutch Connector

M98_MLB

31

ExpressCard Connector

BEN_K20

32

Ethernet PHY (RTL8211CL)

SUMA_K20

33

Ethernet & AirPort Support

SUMA_K20

34

Ethernet Connector

SUMA_K20

35

FireWire LLC/PHY (FW643)

M98_MLB

36

FireWire Port Power

YMU_K20

37

FireWire Ports

M98_MLB

38

SATA Connectors

M98_MLB

39

External USB Connectors

M98_MLB

40

Front Flex Support

CHANG_K20

41

SMC

T18_MLB

42

SMC Support

M98_MLB

43

LPC+SPI Debug Connector

CHANG_K20

44

K20 SMBUS CONNECTIONS

BEN_K20

45

Current & Voltage Sensing

YMU_K20

Page

Contents

Sync

46

Current Sensing

YMU_K20

47

Thermal Sensors

YMU_K20

48

Fan Connectors

M98_MLB

49

WELLSPRING 1

YMA_K20

50

WELLSPRING 2

K20_MLB

51

Sudden Motion Sensor (SMS)

YMU_K20

52

SPI ROM

M98_MLB

53

AUDIO:CODEC

AUDIO_K20

54

AUDIO: LINE IN

AUDIO_K20

55

AUDIO: HEADPHONE AMP

AUDIO_K20

56

AUDIO:SPEAKER AMP

AUDIO_K20

57

AUDIO: JACKS

AUDIO_K20

58

AUDIO: JACK TRANSLATORS

AUDIO_K20

59

DC-In & Battery Connectors

RXU_K20

60

PBus Supply & Battery Charger

RXU_K20

61

IMVP6 CPU VCore Regulator

RXU_K20

62

5V / 3.3V Power Supply

RXU_K20

63

1.5V DDR3 Supply

RXU_K20

64

5V S0 / MCP CORE REGULATOR

RXU_K20

65

CPU VTT Power Supply

RXU_K20

66

Misc Power Supplies

RXU_K20

67

Power Control

YMA_K20

68

Power FETs

YMA_K20

69

NV G96 PCI-E

M98_MLB

70

NV G96 CORE/FB POWER

M98_MLB

71

NV G96 FRAME BUFFER I/F

K20_MLB

72

GDDR3 Frame Buffer A (Bottom)

M98_MLB

73

GDDR3 Frame Buffer B (Bottom)

M98_MLB

74

NV G96 GPIO/MIO/MISC

K20_MLB

75

G96 GPIOs & Straps

M98_MLB

76

NV G96 Video Interfaces

K20_MLB

77

GPU (G96) CORE SUPPLY

RXU_K20

78

LVDS Display Connector

M98_MLB

79

GDDR3 Frame Buffer A (Top)

M99_MLB

80

GDDR3 Frame Buffer B (Top)

M98_MLB

81

Muxed Graphics Support

M98_MLB

82

DisplayPort Connector

K20_MLB

83

1.1V / 1V8 FB Power Supply

RXU_K20

84

Graphics MUX (GMUX)

T18_MXGMUX

85

LCD BACKLIGHT DRIVER

KIRAN_K20

86

LCD Backlight Support

YLEE_K20

87

Misc Power Supplies

RXU_K20

88

CPU/FSB Constraints

M98_MLB

89

Memory Constraints

M98_MLB

90

MCP Constraints 1

M98_MLB

Page

Contents

Sync

91

MCP Constraints 2

M98_MLB

92

Ethernet Constraints

M98_MLB

93

FireWire Constraints

M98_MLB

94

SMC Constraints

M98_MLB

95

GPU (G96) Constraints

M98_MLB

96

Project Specific Constraints

M98_MLB

97

PCB Rule Definitions

M98_MLB

98

PROJECT SPECIFIC CONNS

N/A

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

B

738810

Production Release

DATE

DATE

6/19/09

6/19/09

8

7

6

5

4

3

2

1

06/15/09

Page

Contents

Sync

1

Table of Contents

K20_MLB

2

System Block Diagram

M98_MLB

3

Power Block Diagram

RXU_K20

4

Revision History

NA

5

BOM Configuration

K20A_MLB

6

JTAG Scan Chain

BEN_K20

7

Functional / ICT Test

K20_MLB

8

Power Aliases

RXU_K20

9

Signal Aliases

K20_MLB

10

CPU FSB

M98_MLB

11

CPU Power & Ground

M98_MLB

12

CPU Decoupling & VID

M98_MLB

13

extended Debug Port(MiniXDP)

M98_MLB

14

MCP CPU Interface

T18_MLB

15

MCP Memory Interface

T18_MLB

16

MCP Memory Misc

T18_MLB

17

MCP PCIe Interfaces

T18_MLB

18

MCP Ethernet & Graphics

T18_MLB

19

MCP PCI & LPC

T18_MLB

20

MCP SATA & USB

T18_MLB

21

MCP HDA & MISC

T18_MLB

22

MCP Power & Ground

T18_MLB

23

MCP Standard Decoupling

M98_MLB

24

MCP Graphics Support

M98_MLB

25

SB Misc

M98_MLB

26

FSB/DDR3/FRAMBUF Vref Margining

BEN_K20

27

DDR3 SO-DIMM Connector A

BEN_K20

28

DDR3 SO-DIMM Connector B

BEN_K20

29

DDR3 Support

M98_MLB

30

Right Clutch Connector

M98_MLB

31

ExpressCard Connector

BEN_K20

32

Ethernet PHY (RTL8211CL)

SUMA_K20

33

Ethernet & AirPort Support

SUMA_K20

34

Ethernet Connector

SUMA_K20

35

FireWire LLC/PHY (FW643)

M98_MLB

36

FireWire Port Power

YMU_K20

37

FireWire Ports

M98_MLB

38

SATA Connectors

M98_MLB

39

External USB Connectors

M98_MLB

40

Front Flex Support

CHANG_K20

41

SMC

T18_MLB

42

SMC Support

M98_MLB

43

LPC+SPI Debug Connector

CHANG_K20

44

K20 SMBUS CONNECTIONS

BEN_K20

45

Current & Voltage Sensing

YMU_K20

Page

Contents

Sync

46

Current Sensing

YMU_K20

47

Thermal Sensors

YMU_K20

48

Fan Connectors

M98_MLB

49

WELLSPRING 1

YMA_K20

50

WELLSPRING 2

K20_MLB

51

Sudden Motion Sensor (SMS)

YMU_K20

52

SPI ROM

M98_MLB

53

AUDIO:CODEC

AUDIO_K20

54

AUDIO: LINE IN

AUDIO_K20

55

AUDIO: HEADPHONE AMP

AUDIO_K20

56

AUDIO:SPEAKER AMP

AUDIO_K20

57

AUDIO: JACKS

AUDIO_K20

58

AUDIO: JACK TRANSLATORS

AUDIO_K20

59

DC-In & Battery Connectors

RXU_K20

60

PBus Supply & Battery Charger

RXU_K20

61

IMVP6 CPU VCore Regulator

RXU_K20

62

5V / 3.3V Power Supply

RXU_K20

63

1.5V DDR3 Supply

RXU_K20

64

5V S0 / MCP CORE REGULATOR

RXU_K20

65

CPU VTT Power Supply

RXU_K20

66

Misc Power Supplies

RXU_K20

67

Power Control

YMA_K20

68

Power FETs

YMA_K20

69

NV G96 PCI-E

M98_MLB

70

NV G96 CORE/FB POWER

M98_MLB

71

NV G96 FRAME BUFFER I/F

K20_MLB

72

GDDR3 Frame Buffer A (Bottom)

M98_MLB

73

GDDR3 Frame Buffer B (Bottom)

M98_MLB

74

NV G96 GPIO/MIO/MISC

K20_MLB

75

G96 GPIOs & Straps

M98_MLB

76

NV G96 Video Interfaces

K20_MLB

77

GPU (G96) CORE SUPPLY

RXU_K20

78

LVDS Display Connector

M98_MLB

79

GDDR3 Frame Buffer A (Top)

M99_MLB

80

GDDR3 Frame Buffer B (Top)

M98_MLB

81

Muxed Graphics Support

M98_MLB

82

DisplayPort Connector

K20_MLB

83

1.1V / 1V8 FB Power Supply

RXU_K20

84

Graphics MUX (GMUX)

T18_MXGMUX

85

LCD BACKLIGHT DRIVER

KIRAN_K20

86

LCD Backlight Support

YLEE_K20

87

Misc Power Supplies

RXU_K20

88

CPU/FSB Constraints

M98_MLB

89

Memory Constraints

M98_MLB

90

MCP Constraints 1

M98_MLB

Page

Contents

Sync

91

MCP Constraints 2

M98_MLB

92

Ethernet Constraints

M98_MLB

93

FireWire Constraints

M98_MLB

94

SMC Constraints

M98_MLB

95

GPU (G96) Constraints

M98_MLB

96

Project Specific Constraints

M98_MLB

97

PCB Rule Definitions

M98_MLB

98

PROJECT SPECIFIC CONNS

N/A

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

B

738810

Production Release

DATE

DATE

6/19/09

6/19/09

8

7

6

5

4

3

2

1

06/15/09

Page

Contents

Sync

1

Table of Contents

K20_MLB

2

System Block Diagram

M98_MLB

3

Power Block Diagram

RXU_K20

4

Revision History

NA

5

BOM Configuration

K20A_MLB

6

JTAG Scan Chain

BEN_K20

7

Functional / ICT Test

K20_MLB

8

Power Aliases

RXU_K20

9

Signal Aliases

K20_MLB

10

CPU FSB

M98_MLB

11

CPU Power & Ground

M98_MLB

12

CPU Decoupling & VID

M98_MLB

13

extended Debug Port(MiniXDP)

M98_MLB

14

MCP CPU Interface

T18_MLB

15

MCP Memory Interface

T18_MLB

16

MCP Memory Misc

T18_MLB

17

MCP PCIe Interfaces

T18_MLB

18

MCP Ethernet & Graphics

T18_MLB

19

MCP PCI & LPC

T18_MLB

20

MCP SATA & USB

T18_MLB

21

MCP HDA & MISC

T18_MLB

22

MCP Power & Ground

T18_MLB

23

MCP Standard Decoupling

M98_MLB

24

MCP Graphics Support

M98_MLB

25

SB Misc

M98_MLB

26

FSB/DDR3/FRAMBUF Vref Margining

BEN_K20

27

DDR3 SO-DIMM Connector A

BEN_K20

28

DDR3 SO-DIMM Connector B

BEN_K20

29

DDR3 Support

M98_MLB

30

Right Clutch Connector

M98_MLB

31

ExpressCard Connector

BEN_K20

32

Ethernet PHY (RTL8211CL)

SUMA_K20

33

Ethernet & AirPort Support

SUMA_K20

34

Ethernet Connector

SUMA_K20

35

FireWire LLC/PHY (FW643)

M98_MLB

36

FireWire Port Power

YMU_K20

37

FireWire Ports

M98_MLB

38

SATA Connectors

M98_MLB

39

External USB Connectors

M98_MLB

40

Front Flex Support

CHANG_K20

41

SMC

T18_MLB

42

SMC Support

M98_MLB

43

LPC+SPI Debug Connector

CHANG_K20

44

K20 SMBUS CONNECTIONS

BEN_K20

45

Current & Voltage Sensing

YMU_K20

Page

Contents

Sync

46

Current Sensing

YMU_K20

47

Thermal Sensors

YMU_K20

48

Fan Connectors

M98_MLB

49

WELLSPRING 1

YMA_K20

50

WELLSPRING 2

K20_MLB

51

Sudden Motion Sensor (SMS)

YMU_K20

52

SPI ROM

M98_MLB

53

AUDIO:CODEC

AUDIO_K20

54

AUDIO: LINE IN

AUDIO_K20

55

AUDIO: HEADPHONE AMP

AUDIO_K20

56

AUDIO:SPEAKER AMP

AUDIO_K20

57

AUDIO: JACKS

AUDIO_K20

58

AUDIO: JACK TRANSLATORS

AUDIO_K20

59

DC-In & Battery Connectors

RXU_K20

60

PBus Supply & Battery Charger

RXU_K20

61

IMVP6 CPU VCore Regulator

RXU_K20

62

5V / 3.3V Power Supply

RXU_K20

63

1.5V DDR3 Supply

RXU_K20

64

5V S0 / MCP CORE REGULATOR

RXU_K20

65

CPU VTT Power Supply

RXU_K20

66

Misc Power Supplies

RXU_K20

67

Power Control

YMA_K20

68

Power FETs

YMA_K20

69

NV G96 PCI-E

M98_MLB

70

NV G96 CORE/FB POWER

M98_MLB

71

NV G96 FRAME BUFFER I/F

K20_MLB

72

GDDR3 Frame Buffer A (Bottom)

M98_MLB

73

GDDR3 Frame Buffer B (Bottom)

M98_MLB

74

NV G96 GPIO/MIO/MISC

K20_MLB

75

G96 GPIOs & Straps

M98_MLB

76

NV G96 Video Interfaces

K20_MLB

77

GPU (G96) CORE SUPPLY

RXU_K20

78

LVDS Display Connector

M98_MLB

79

GDDR3 Frame Buffer A (Top)

M99_MLB

80

GDDR3 Frame Buffer B (Top)

M98_MLB

81

Muxed Graphics Support

M98_MLB

82

DisplayPort Connector

K20_MLB

83

1.1V / 1V8 FB Power Supply

RXU_K20

84

Graphics MUX (GMUX)

T18_MXGMUX

85

LCD BACKLIGHT DRIVER

KIRAN_K20

86

LCD Backlight Support

YLEE_K20

87

Misc Power Supplies

RXU_K20

88

CPU/FSB Constraints

M98_MLB

89

Memory Constraints

M98_MLB

90

MCP Constraints 1

M98_MLB

Page

Contents

Sync

91

MCP Constraints 2

M98_MLB

92

Ethernet Constraints

M98_MLB

93

FireWire Constraints

M98_MLB

94

SMC Constraints

M98_MLB

95

GPU (G96) Constraints

M98_MLB

96

Project Specific Constraints

M98_MLB

97

PCB Rule Definitions

M98_MLB

98

PROJECT SPECIFIC CONNS

N/A

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

B

738810

Production Release

DATE

DATE

6/19/09

6/19/09

8

7

6

5

4

3

2

1

06/15/09

Page

Contents

Sync

1

Table of Contents

K20_MLB

2

System Block Diagram

M98_MLB

3

Power Block Diagram

RXU_K20

4

Revision History

NA

5

BOM Configuration

K20A_MLB

6

JTAG Scan Chain

BEN_K20

7

Functional / ICT Test

K20_MLB

8

Power Aliases

RXU_K20

9

Signal Aliases

K20_MLB

10

CPU FSB

M98_MLB

11

CPU Power & Ground

M98_MLB

12

CPU Decoupling & VID

M98_MLB

13

extended Debug Port(MiniXDP)

M98_MLB

14

MCP CPU Interface

T18_MLB

15

MCP Memory Interface

T18_MLB

16

MCP Memory Misc

T18_MLB

17

MCP PCIe Interfaces

T18_MLB

18

MCP Ethernet & Graphics

T18_MLB

19

MCP PCI & LPC

T18_MLB

20

MCP SATA & USB

T18_MLB

21

MCP HDA & MISC

T18_MLB

22

MCP Power & Ground

T18_MLB

23

MCP Standard Decoupling

M98_MLB

24

MCP Graphics Support

M98_MLB

25

SB Misc

M98_MLB

26

FSB/DDR3/FRAMBUF Vref Margining

BEN_K20

27

DDR3 SO-DIMM Connector A

BEN_K20

28

DDR3 SO-DIMM Connector B

BEN_K20

29

DDR3 Support

M98_MLB

30

Right Clutch Connector

M98_MLB

31

ExpressCard Connector

BEN_K20

32

Ethernet PHY (RTL8211CL)

SUMA_K20

33

Ethernet & AirPort Support

SUMA_K20

34

Ethernet Connector

SUMA_K20

35

FireWire LLC/PHY (FW643)

M98_MLB

36

FireWire Port Power

YMU_K20

37

FireWire Ports

M98_MLB

38

SATA Connectors

M98_MLB

39

External USB Connectors

M98_MLB

40

Front Flex Support

CHANG_K20

41

SMC

T18_MLB

42

SMC Support

M98_MLB

43

LPC+SPI Debug Connector

CHANG_K20

44

K20 SMBUS CONNECTIONS

BEN_K20

45

Current & Voltage Sensing

YMU_K20

Page

Contents

Sync

46

Current Sensing

YMU_K20

47

Thermal Sensors

YMU_K20

48

Fan Connectors

M98_MLB

49

WELLSPRING 1

YMA_K20

50

WELLSPRING 2

K20_MLB

51

Sudden Motion Sensor (SMS)

YMU_K20

52

SPI ROM

M98_MLB

53

AUDIO:CODEC

AUDIO_K20

54

AUDIO: LINE IN

AUDIO_K20

55

AUDIO: HEADPHONE AMP

AUDIO_K20

56

AUDIO:SPEAKER AMP

AUDIO_K20

57

AUDIO: JACKS

AUDIO_K20

58

AUDIO: JACK TRANSLATORS

AUDIO_K20

59

DC-In & Battery Connectors

RXU_K20

60

PBus Supply & Battery Charger

RXU_K20

61

IMVP6 CPU VCore Regulator

RXU_K20

62

5V / 3.3V Power Supply

RXU_K20

63

1.5V DDR3 Supply

RXU_K20

64

5V S0 / MCP CORE REGULATOR

RXU_K20

65

CPU VTT Power Supply

RXU_K20

66

Misc Power Supplies

RXU_K20

67

Power Control

YMA_K20

68

Power FETs

YMA_K20

69

NV G96 PCI-E

M98_MLB

70

NV G96 CORE/FB POWER

M98_MLB

71

NV G96 FRAME BUFFER I/F

K20_MLB

72

GDDR3 Frame Buffer A (Bottom)

M98_MLB

73

GDDR3 Frame Buffer B (Bottom)

M98_MLB

74

NV G96 GPIO/MIO/MISC

K20_MLB

75

G96 GPIOs & Straps

M98_MLB

76

NV G96 Video Interfaces

K20_MLB

77

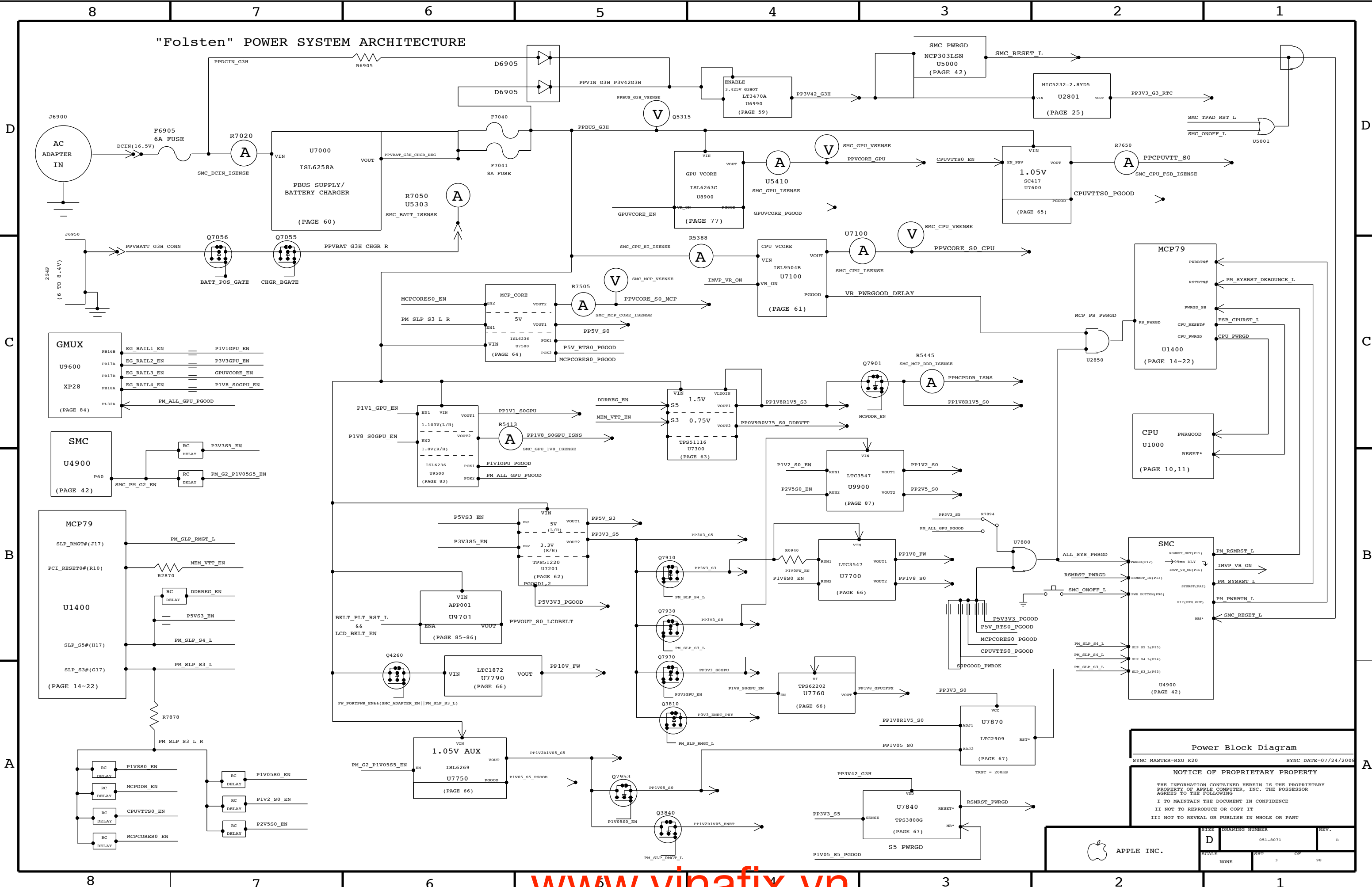
GPU (G96) CORE SUPPLY

RXU_K20

78

LVDS Display Connector





87654321

PVT:

03/24/09
csa.5: Project copied from K20 mlb_pvt.
Changed CPU APNs for 2.8 and 3.06GHz CPUs.
Changed BOM and EEE codes for K20A.
csa.45: Connected =PP1V5_EXP_S0 to J4501.13 for SATA redriver on flex.
03/25/09
csa.9: Added PBUS VS 5V voltage selection resistors for keyboard backlight driver.
03/27/09
csa.90: Added 1000pF cap to the backlight power pin for EMI baseline noise.
03/30/09
csa.5: Changed the bom option to KBDLED_5V per radar# 6723272.
03/31/09
csa.1: Changed rev to 1.0.0
04/09/09
csa.70: No stuff C7099 per radar# 6772695.
04/29/09
Production Release Fab to rev A
csa.5: Changed K20A EFI ROM APN 341S2507 (BOM change only)
05/05/09
Added 128S0264 (SANYO) as alternate to 128S0257 (KEMET ELEC) per Radar# 6656624.
06/15/09
Added 107S0136 (DALE/VISHAY) as alternate to 107S0132 (CYNTEC) per Radar# 6971400.
For U7871 P/N 353S2718 is made primary. P/N 353S2310 is added back as alternate.
For U6100 Locked Bootrom P/N 341S2506 replaces existing Unlock Bootrom P/N 341S2507.

D

C

B

A

87654321

Revision History

SYNC_MASTER=NA SYNC_DATE=NA

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D

SCALE

NONE

SBT

4

OF

98

SIZE

DRAWING NUMBER

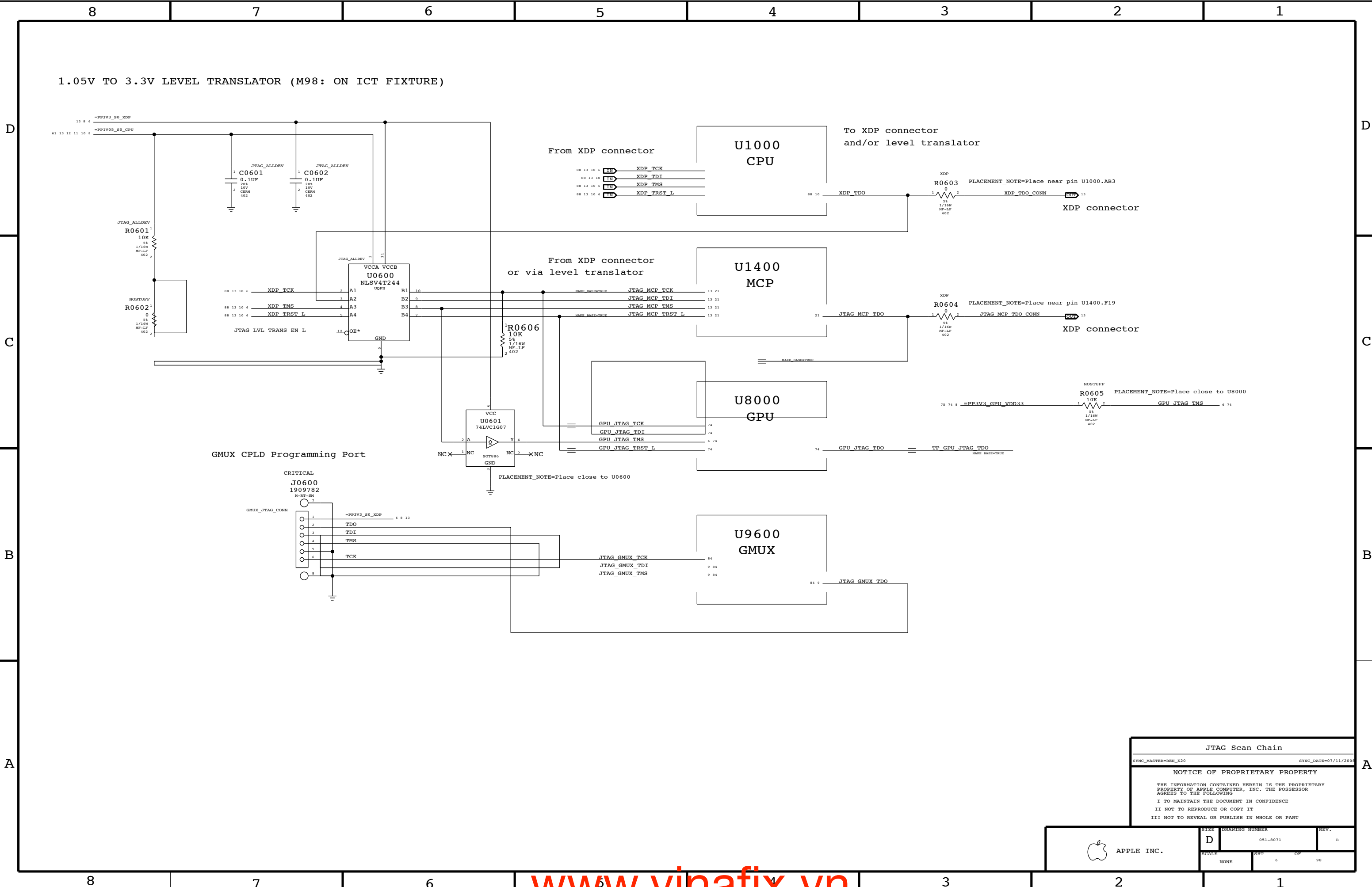
REV.

051-8071

B

87654321

www.vinafix.vn



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

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SIZE: D

DRAWING NUMBER: 051-8071

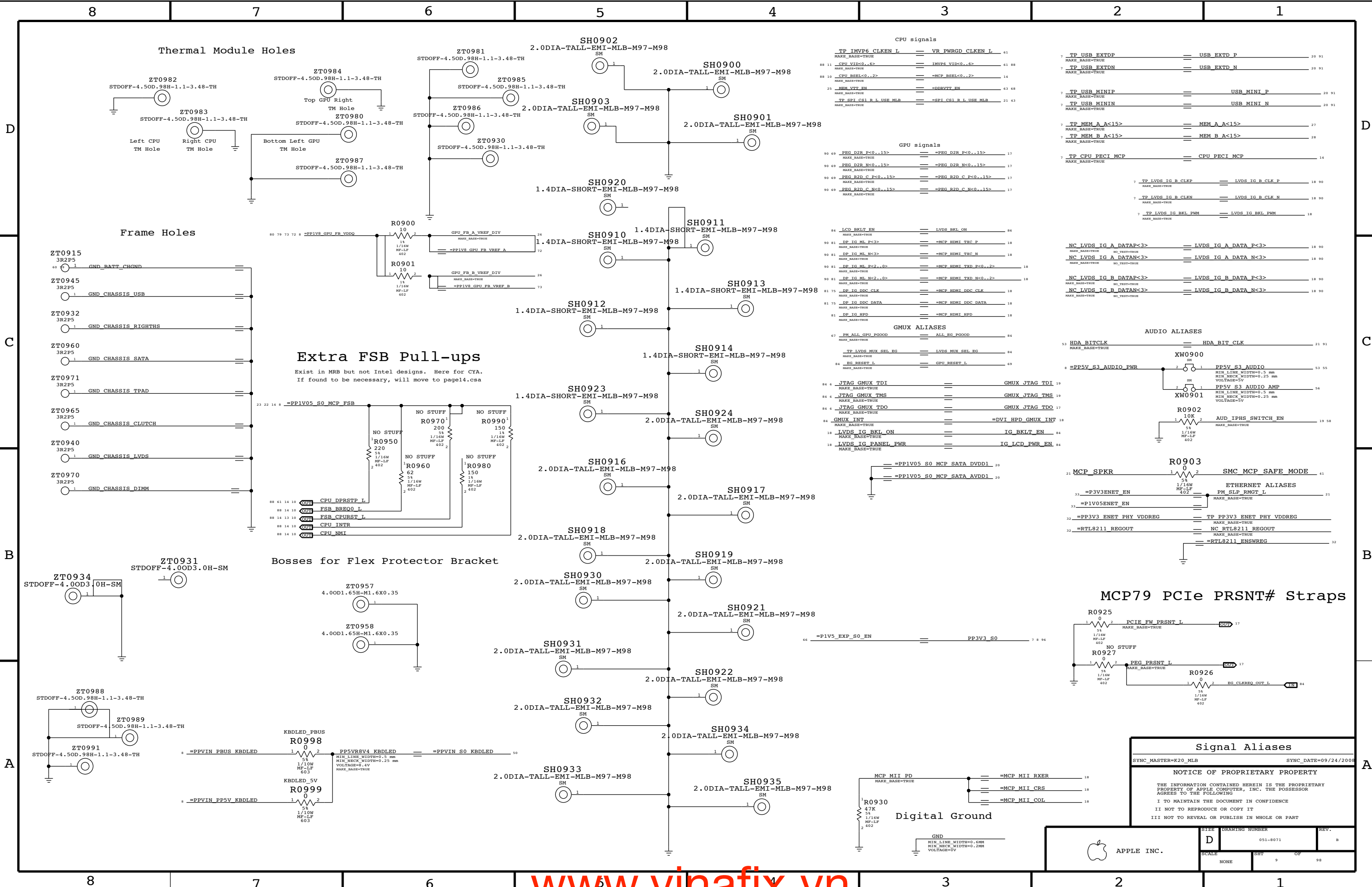
REV.: B

SCALE: NONE

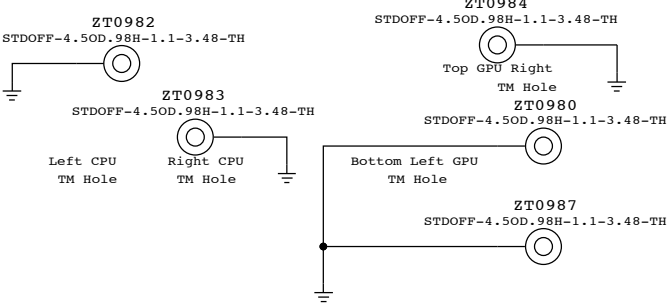
SHT: 6

OF: 98

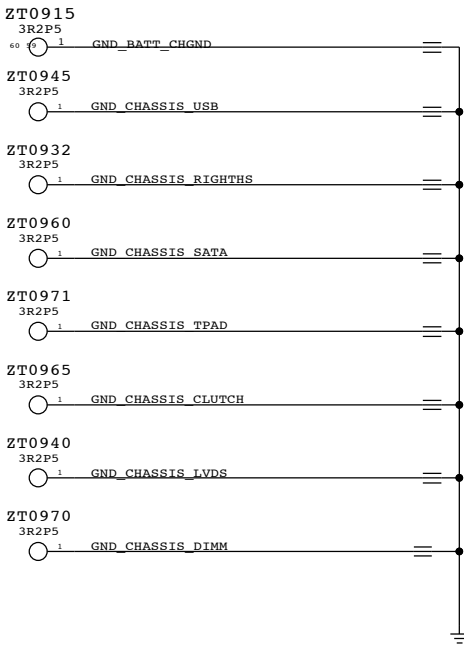




Thermal Module Holes

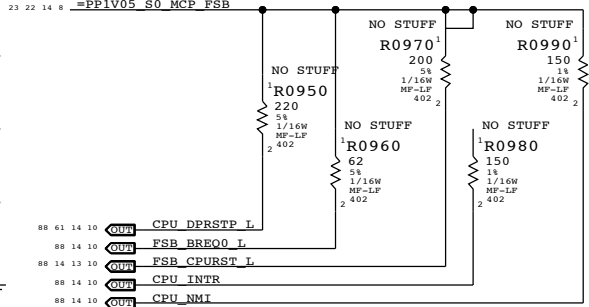


Frame Holes

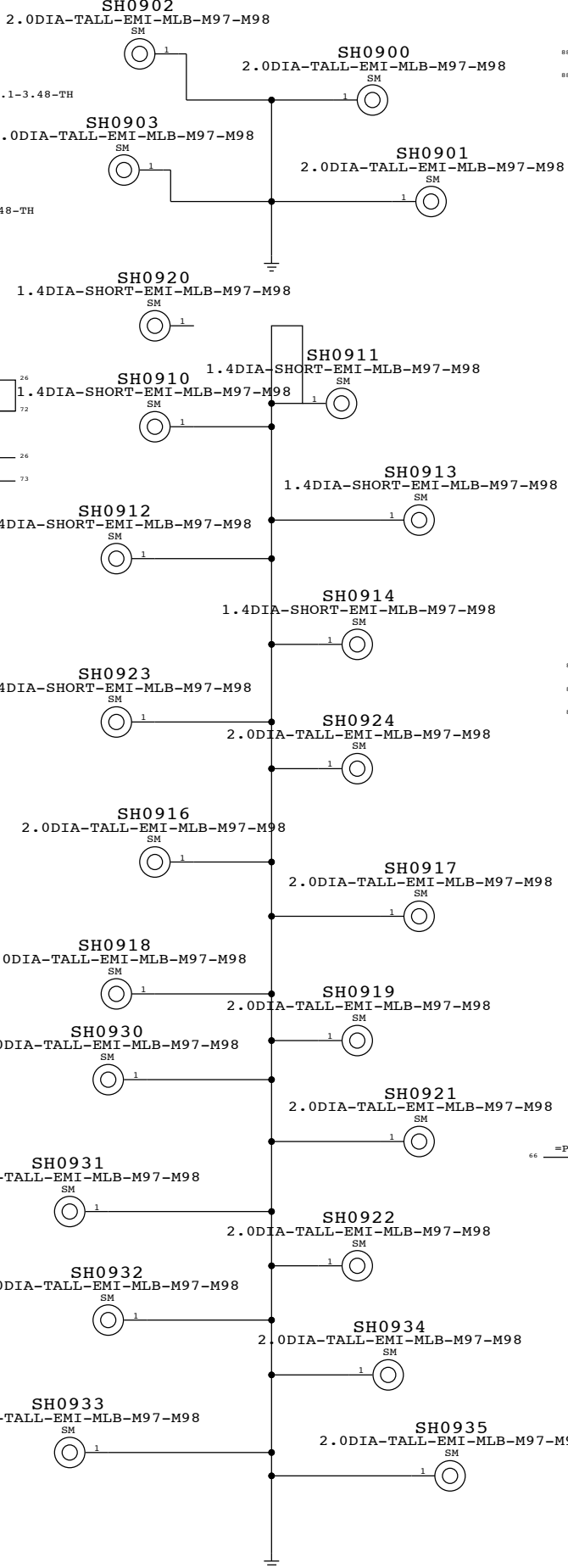
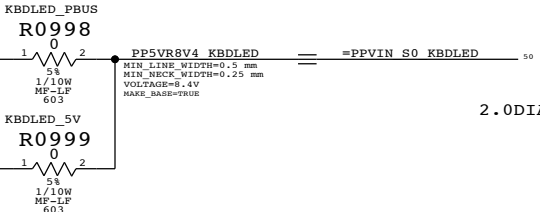
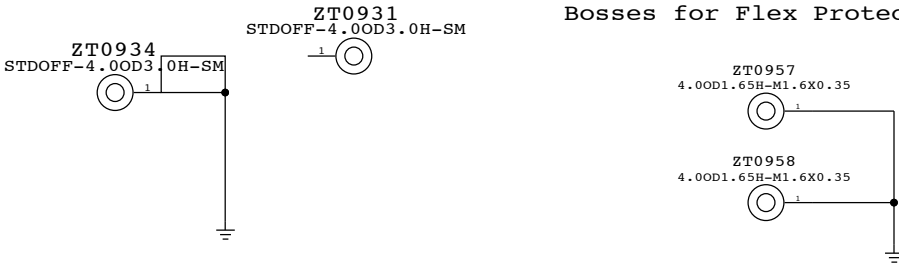


Extra FSB Pull-ups

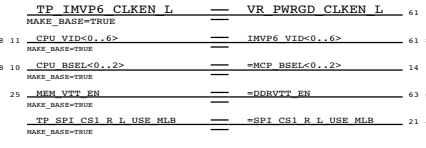
Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to pagel4.csa



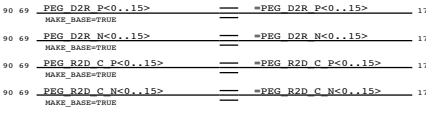
Bosses for Flex Protector Bracket



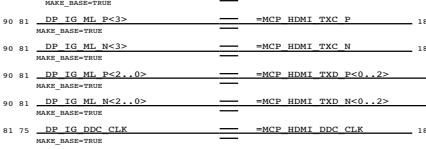
CPU signals



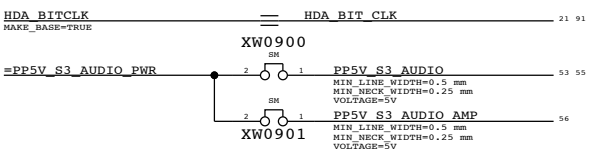
GPU signals



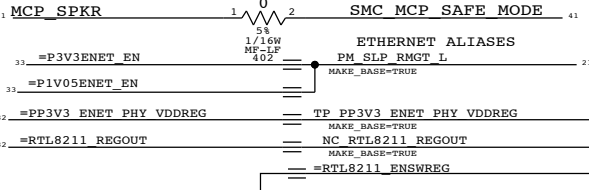
GMUX ALIASES



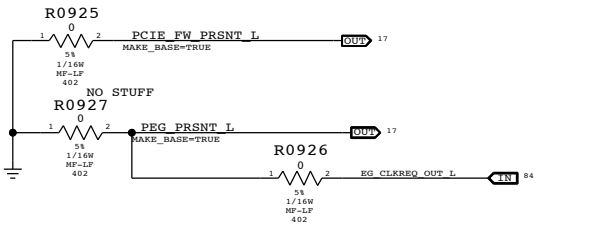
AUDIO ALIASES



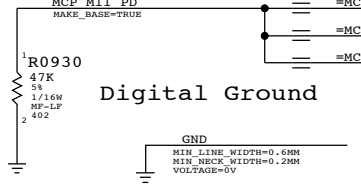
ETHERNET ALIASES



MCP79 PCIe PRSNT# Straps



Digital Ground



Signal Aliases

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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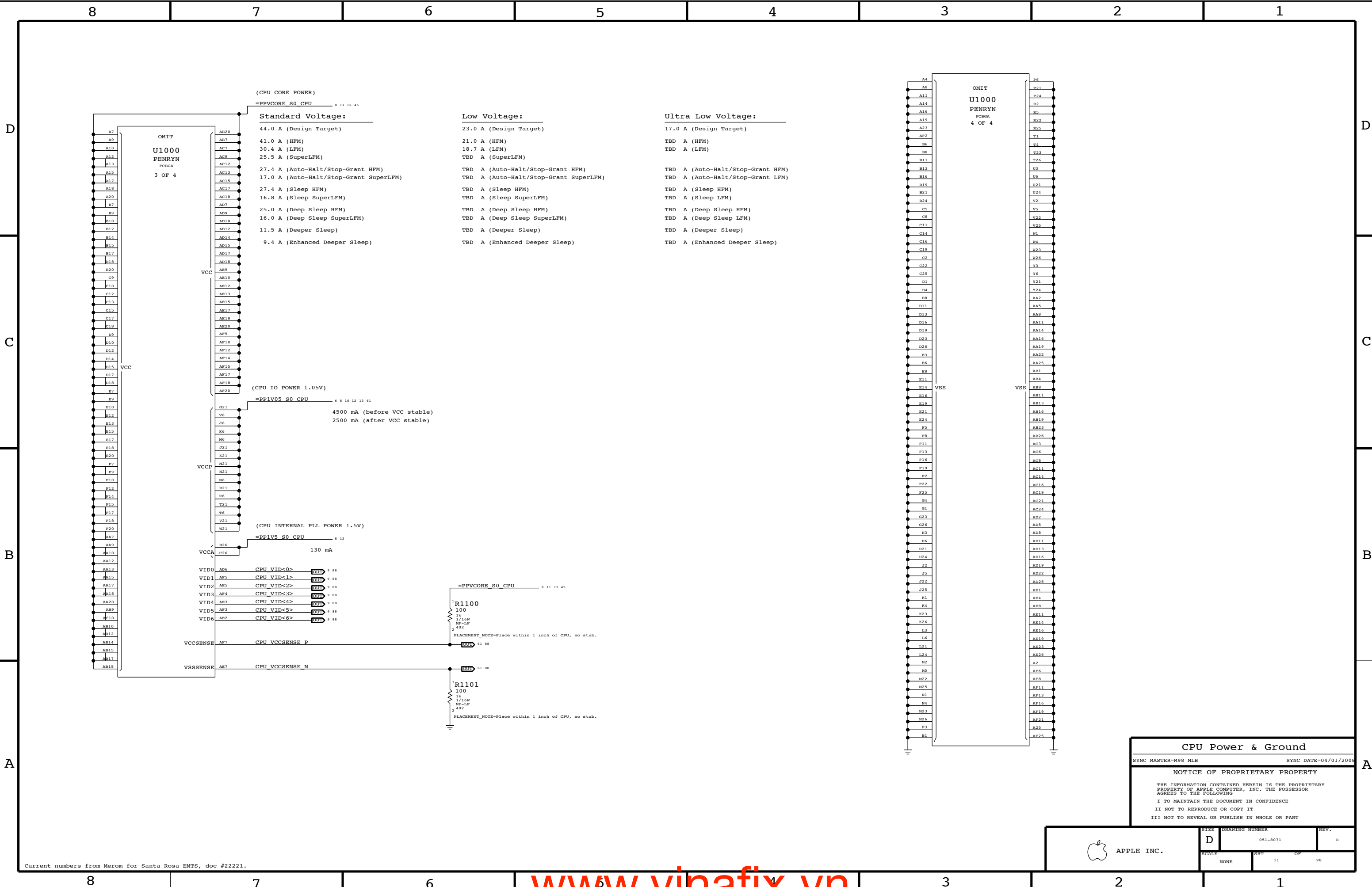
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SCALE	SHT	OF
NONE	9	98





Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=M98_MLB

SYNC_DATE=04/01/2008

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SCALE

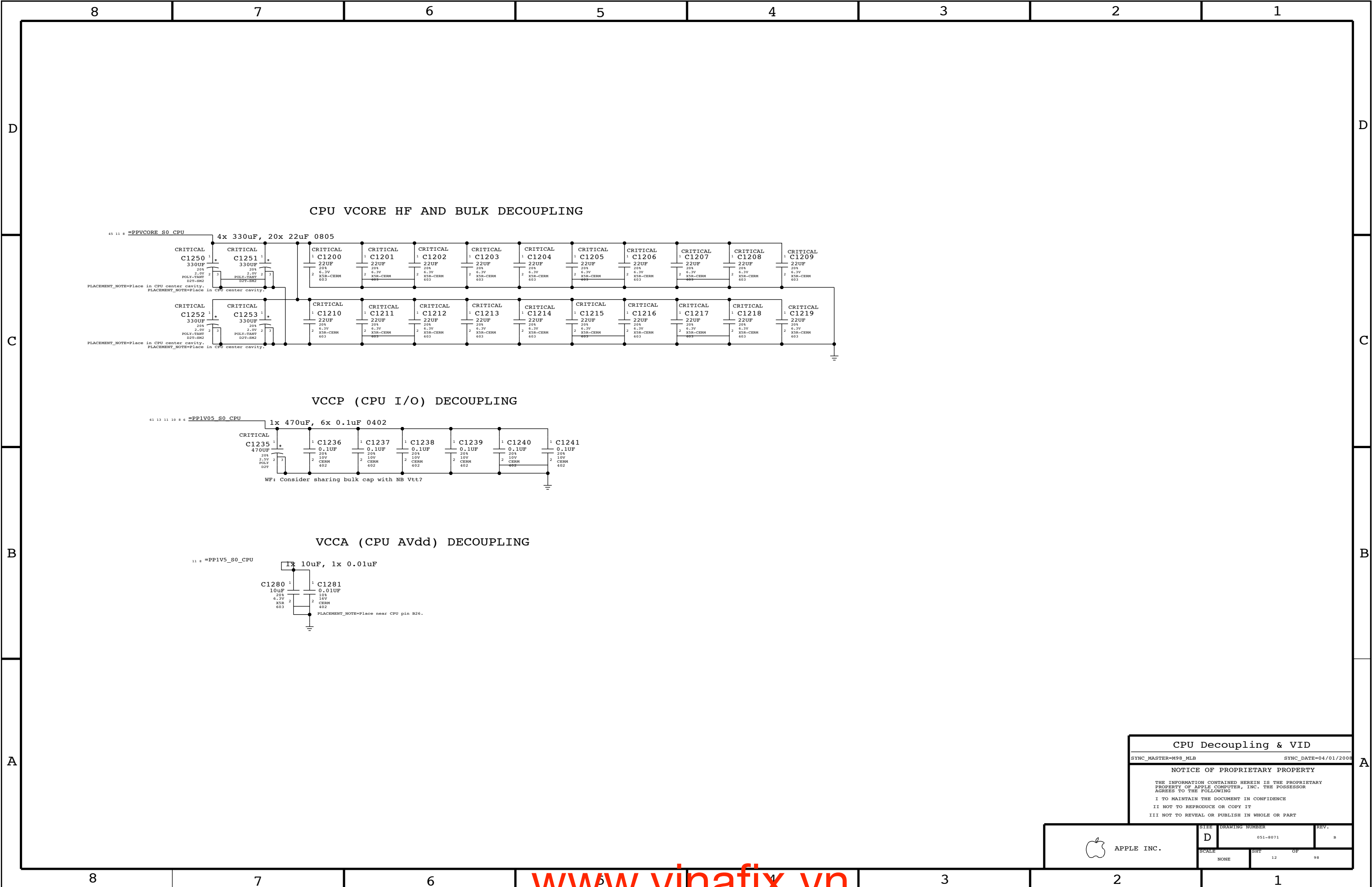
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SBT

11

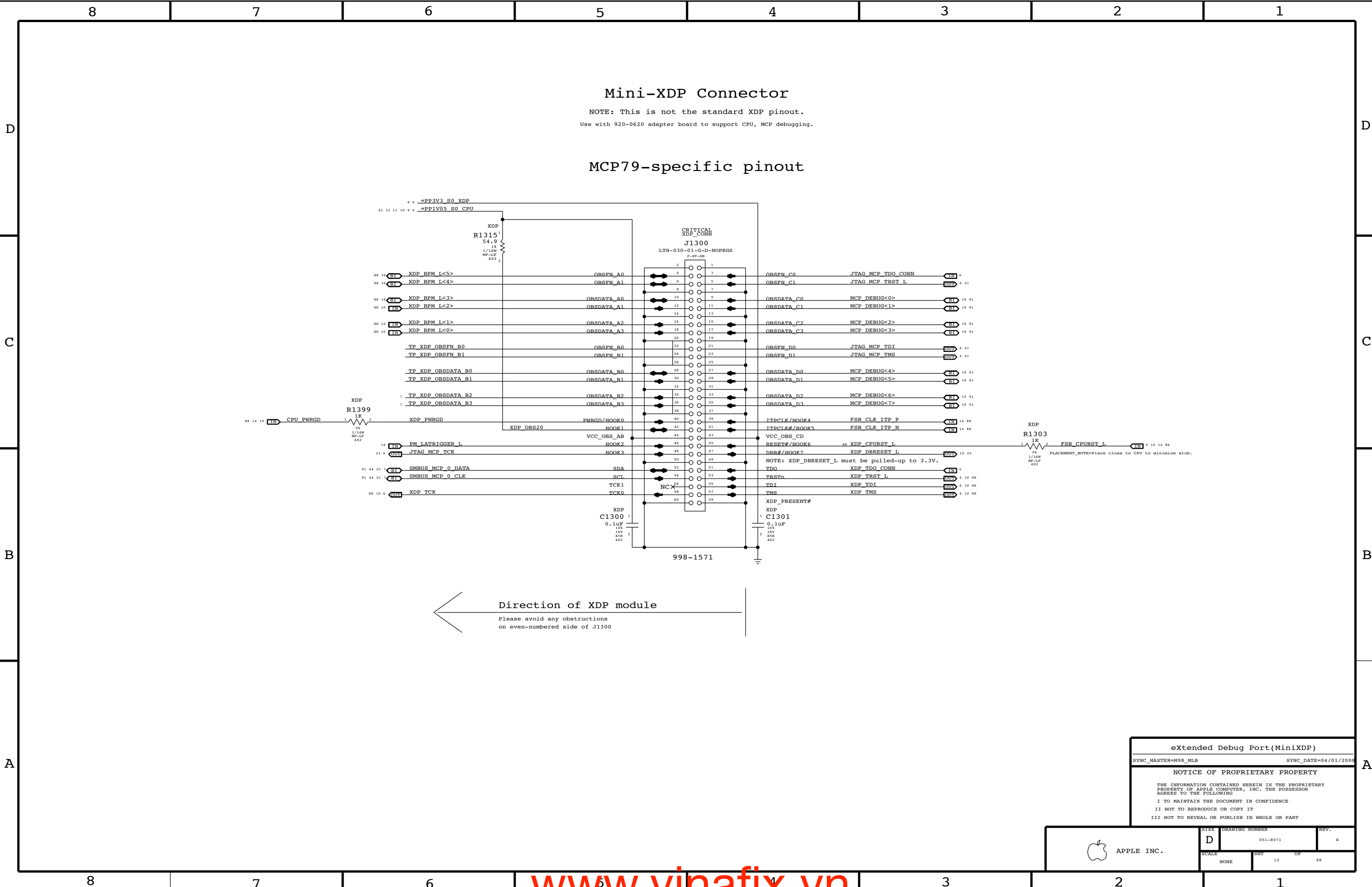
OF

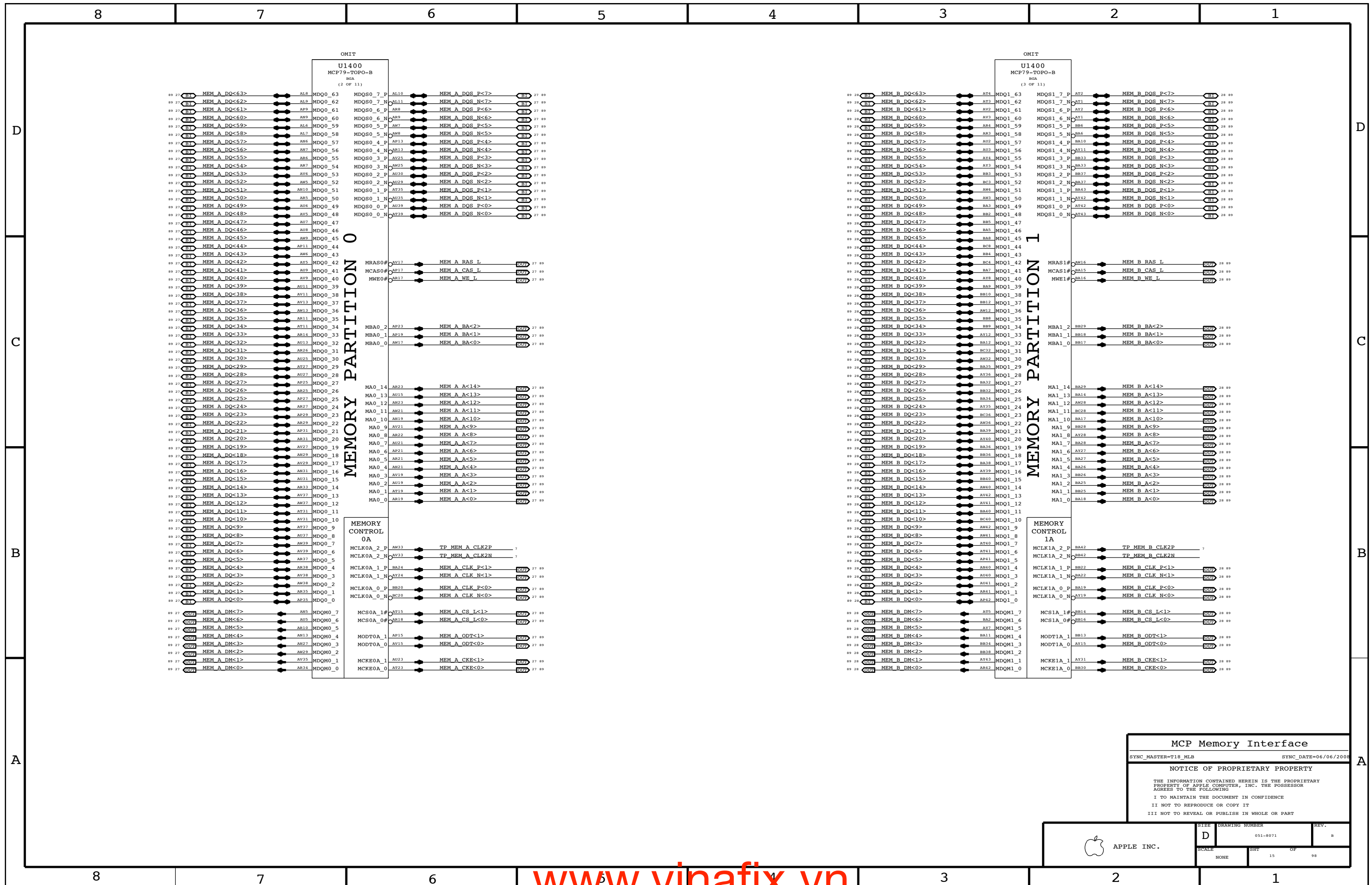
98



CPU Decoupling & VID		
SYNC_MASTER=M98_MLB		SYNC_DATE=04/01/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8071	B
SCALE	NONE	SBT	12 OF 98





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B

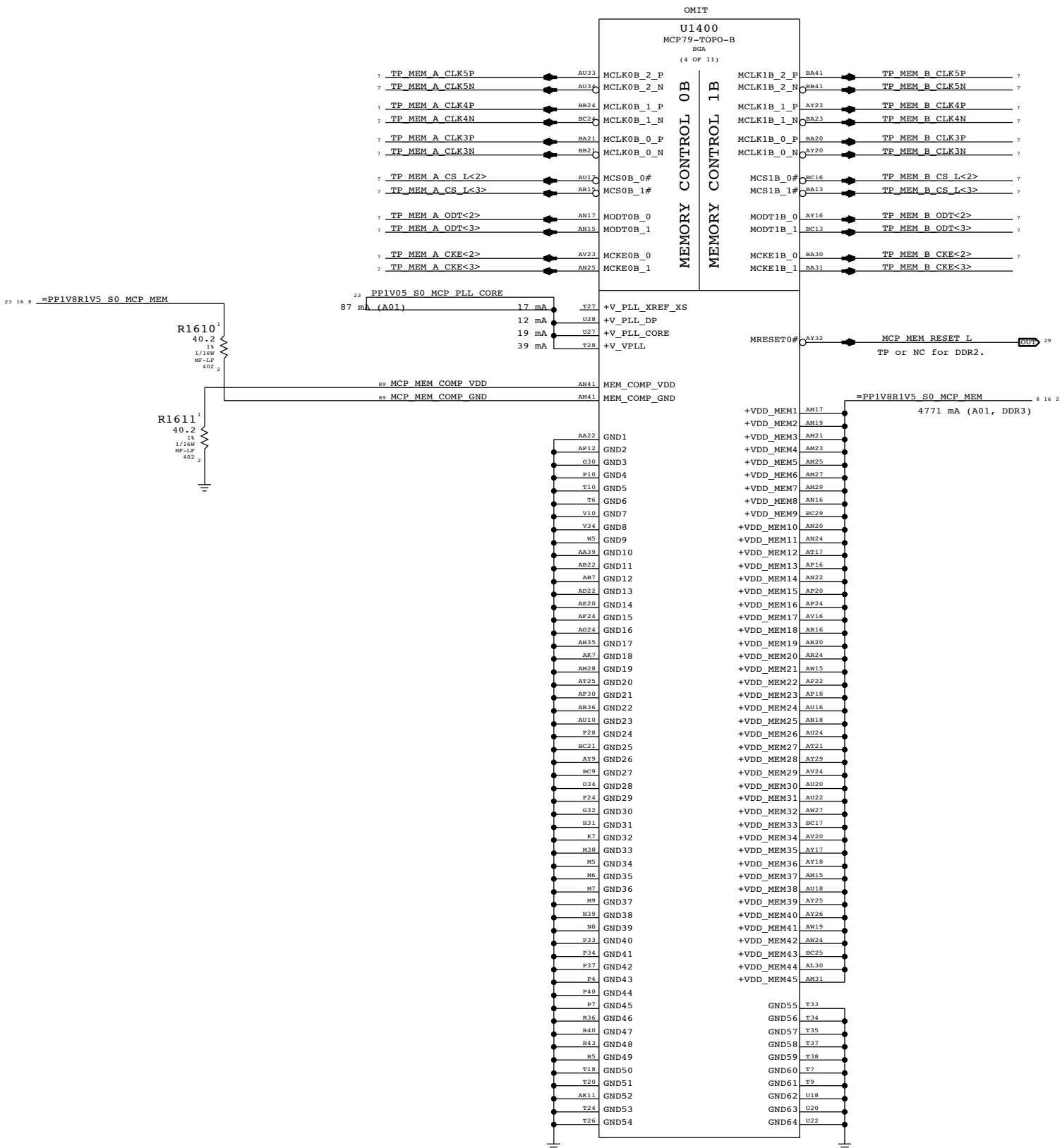
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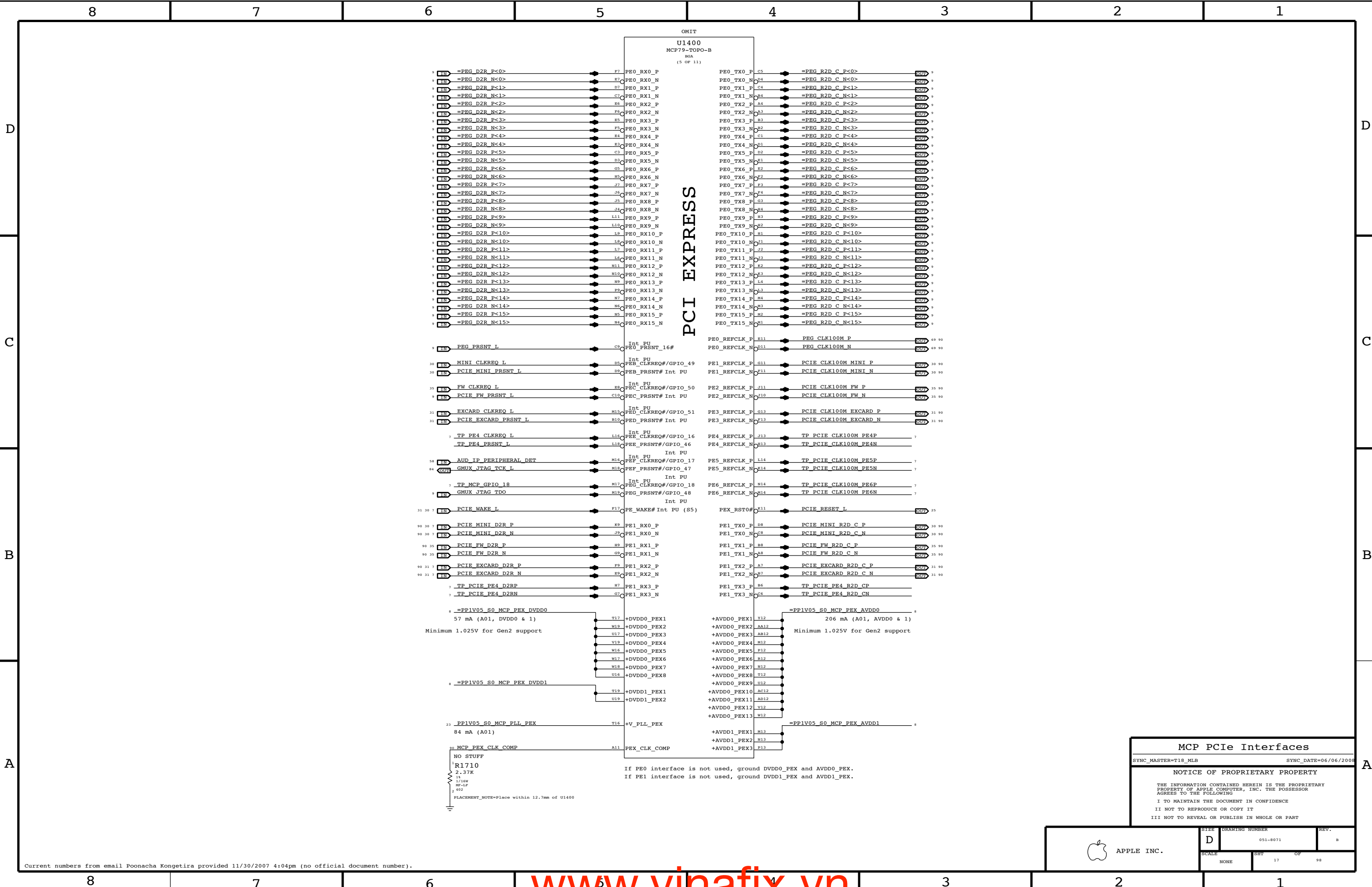
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MCP Memory Misc			
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SCALE	NONE	SBT	16	OF 98



MCP PCIe Interfaces

SYNC_MASTER=T18_MLB

SYNC_DATE=06/06/2008

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SCALE
NONE

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DRAWING NUMBER
051-8071

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17

OF
98

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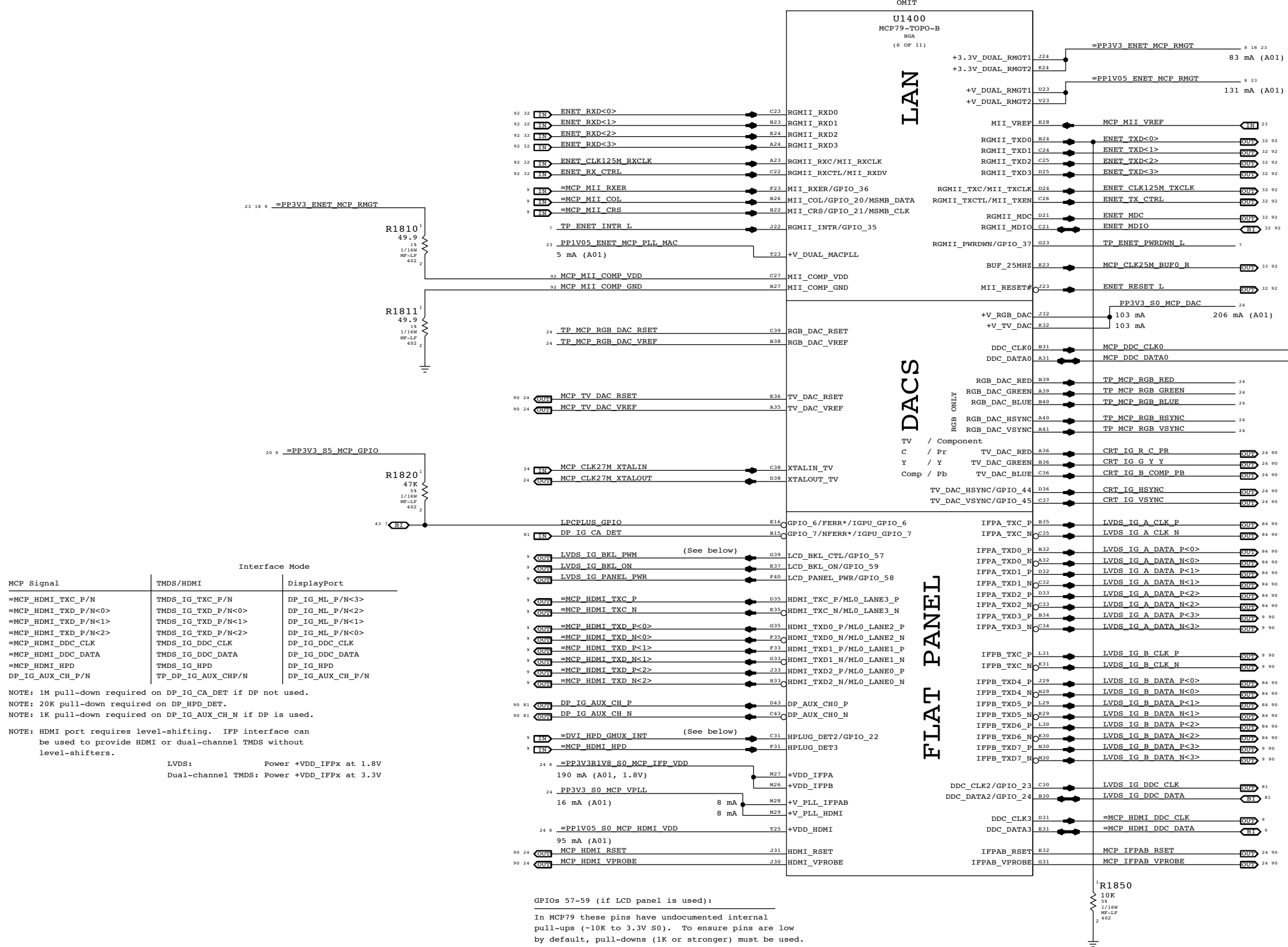
A

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A



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

APPLE INC.

SIZE

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SCALE

NONE

DRAWING NUMBER

051-8071

REV.

B

SCALE

NONE

SBT

18

OF

98

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB

SYNC_DATE=06/06/2008

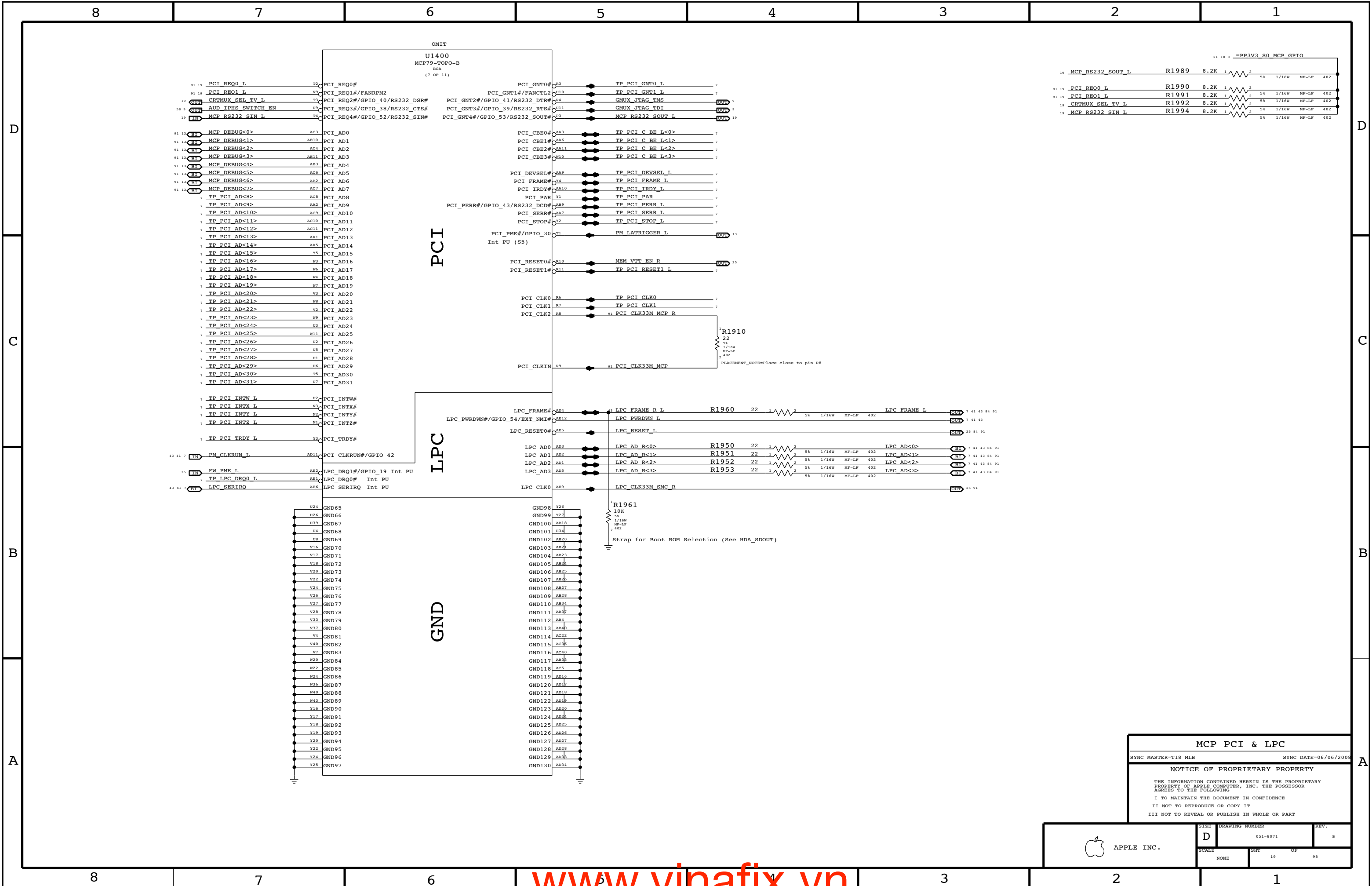
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MCP PCI & LPC

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SIZE: D

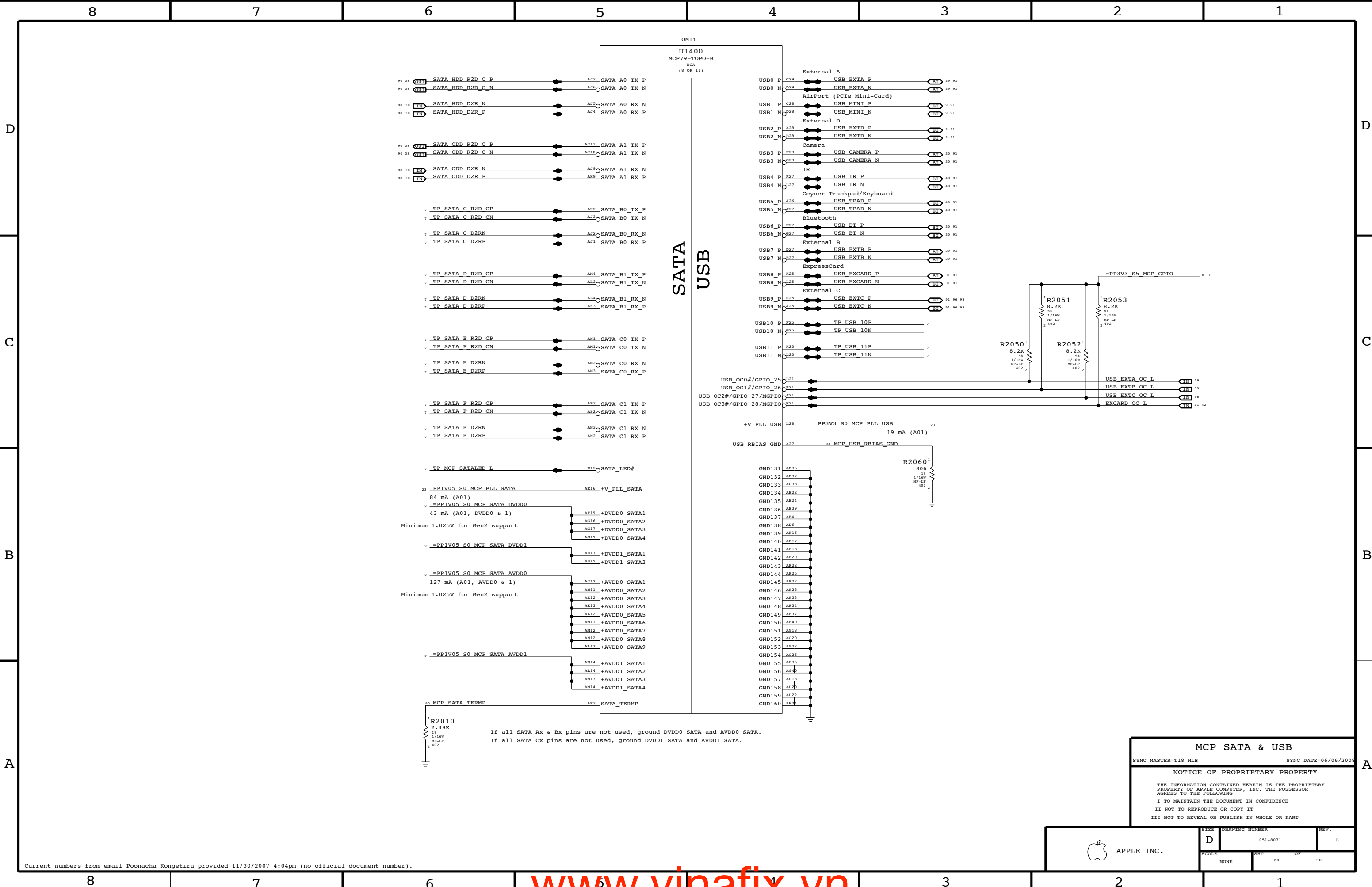
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REV.: B

SCALE: NONE

SBT: 19

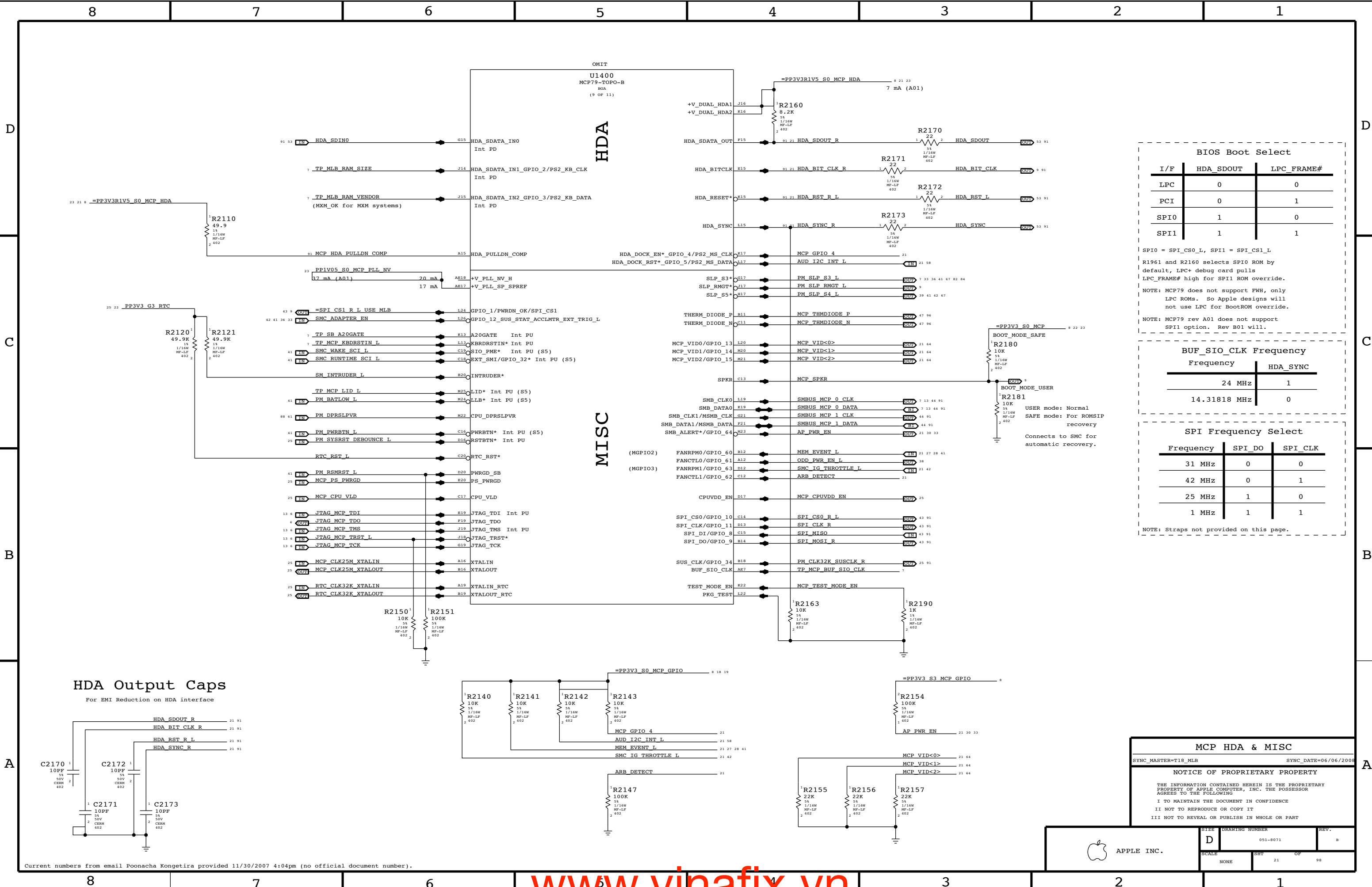
OF: 98



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB	
SYNC_MASTER=T18_MLB	SYNC_DATE=06/06/2008
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	D	051-8071	B
SCALE		20	OF 98



BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

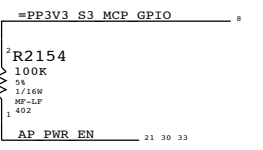
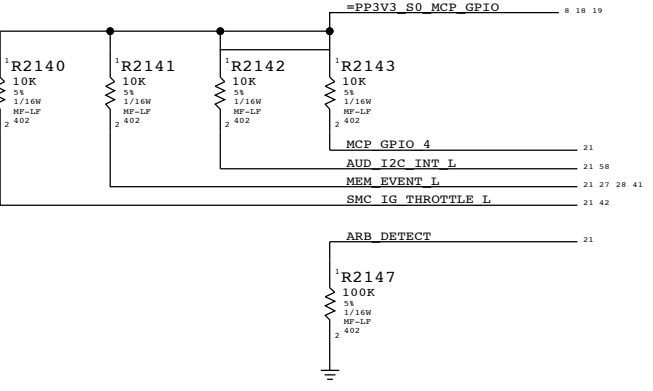
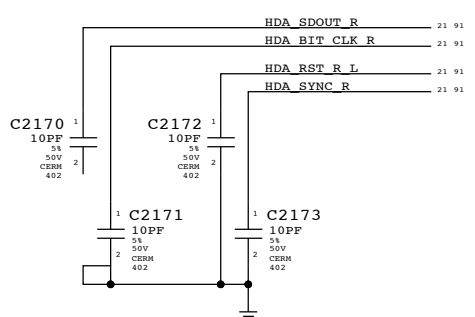
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

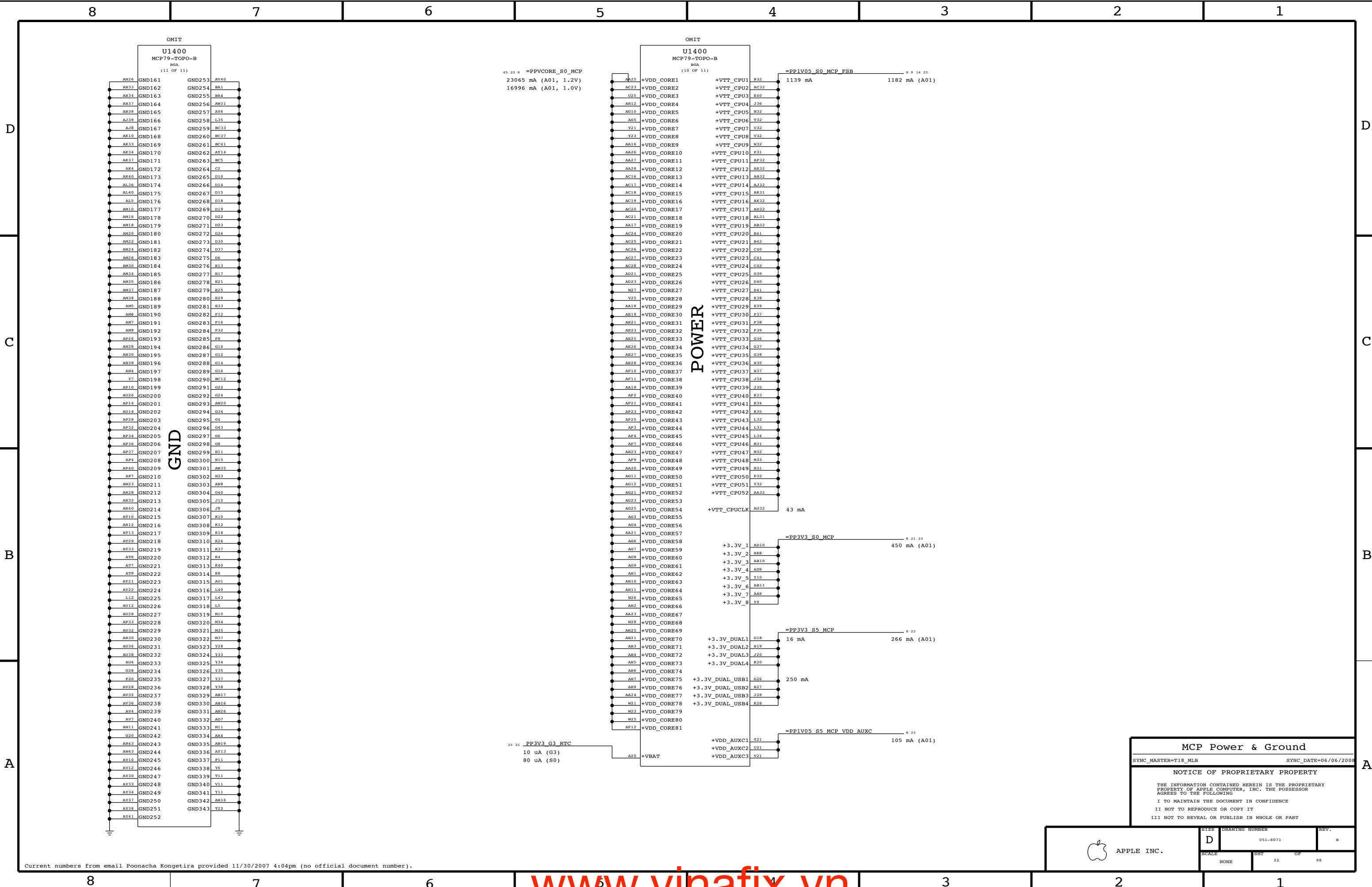
For EMI Reduction on HDA interface



MCP HDA & MISC	
SYNC_MASTER=T18_MLB	SYNC_DATE=06/06/2008
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D	051-8071	B
SCALE		OF
NONE	21	98





Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

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SYNC_DATE=06/06/2008

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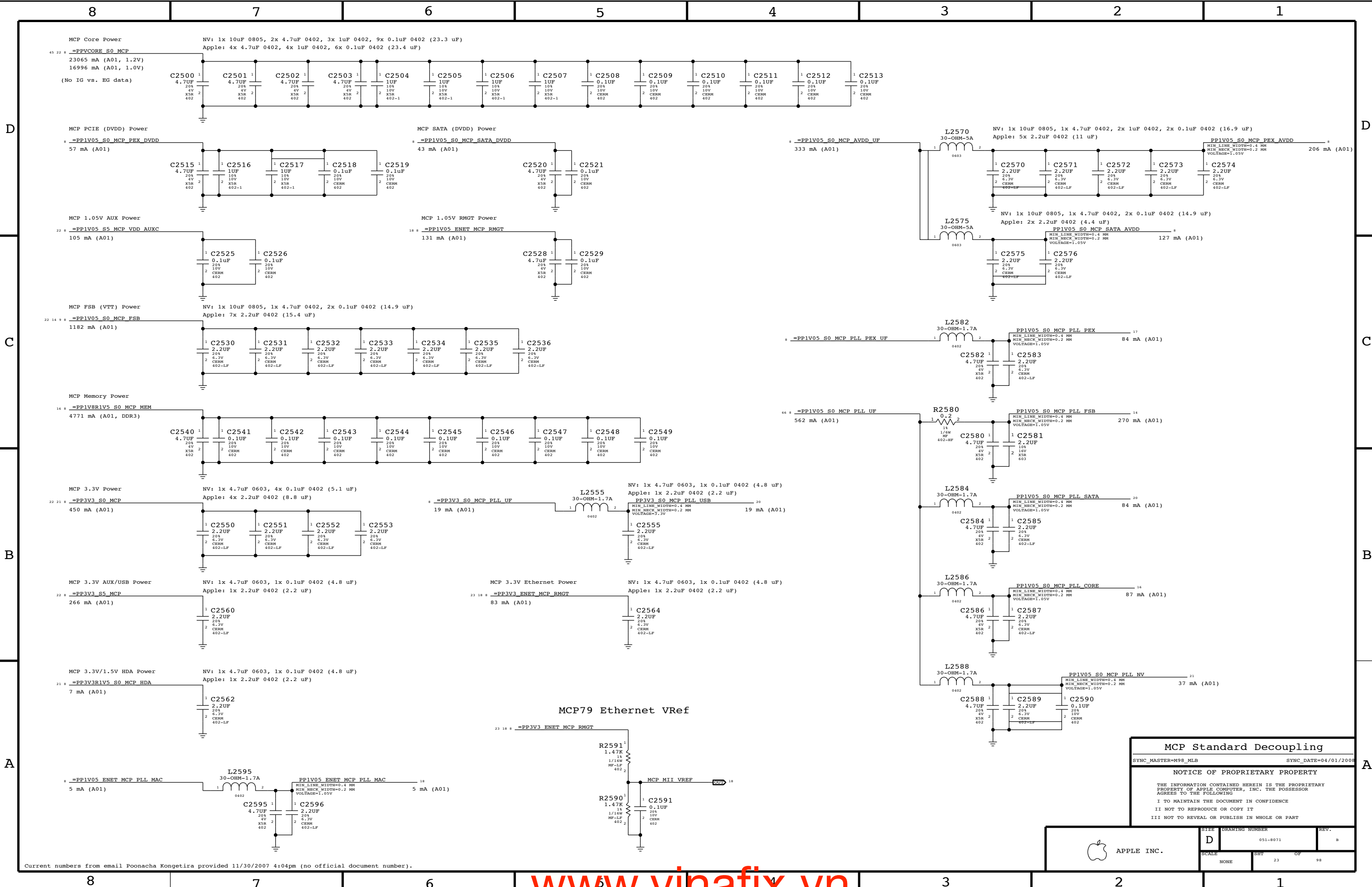
SCALE
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D
DRAWING NUMBER
051-8071

REV.
B

22

OF
98



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB

SYNC_DATE=04/01/2008


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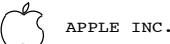
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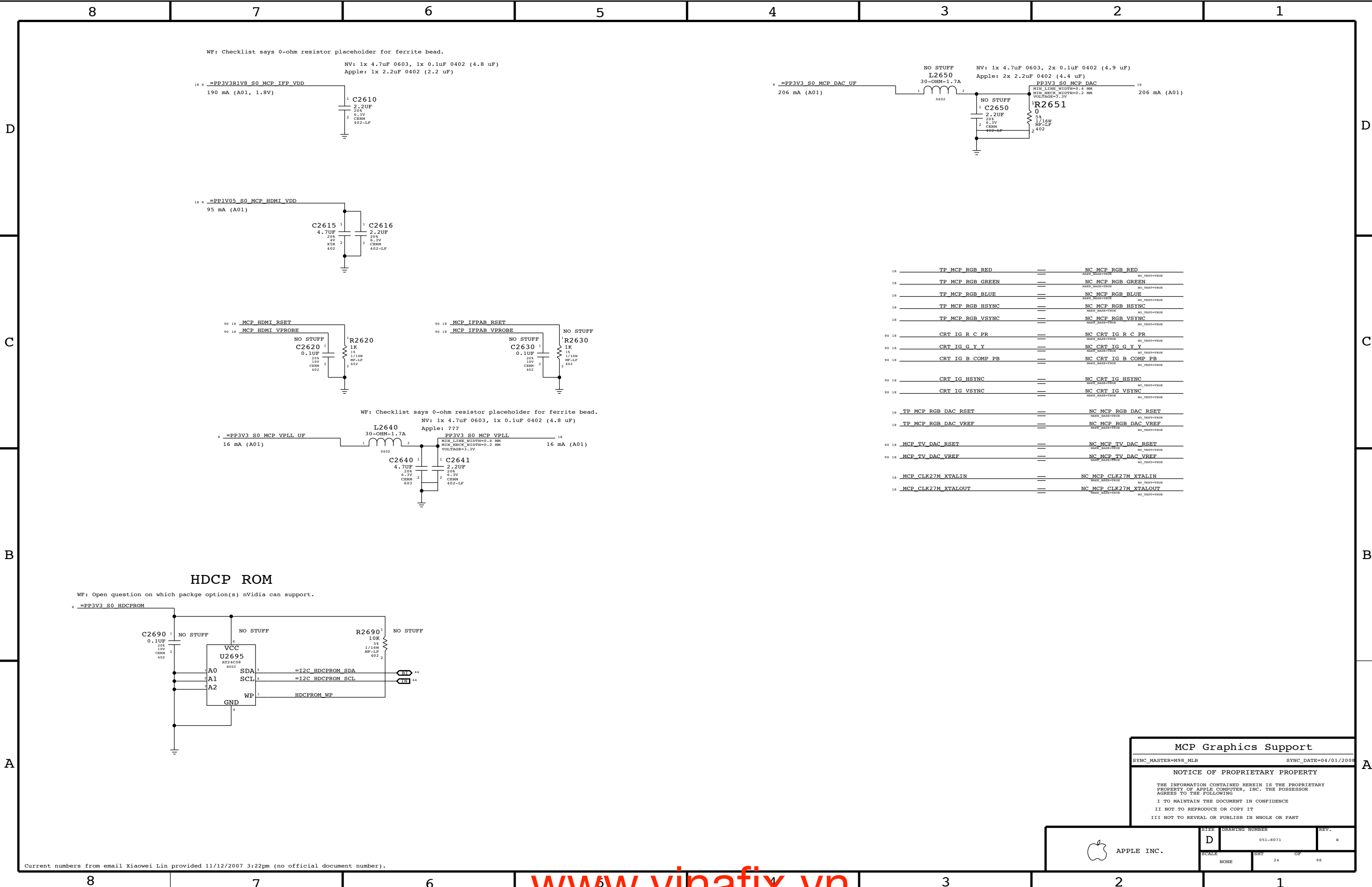
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	D	051-8071		B
	SCALE	SHT OF		
	NONE	23 98		





Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

MCP Graphics Support

SYNC_MASTER=M98_MLB

SYNC_DATE=04/01/2008


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SIZE: D

DRAWING NUMBER: 051-8071

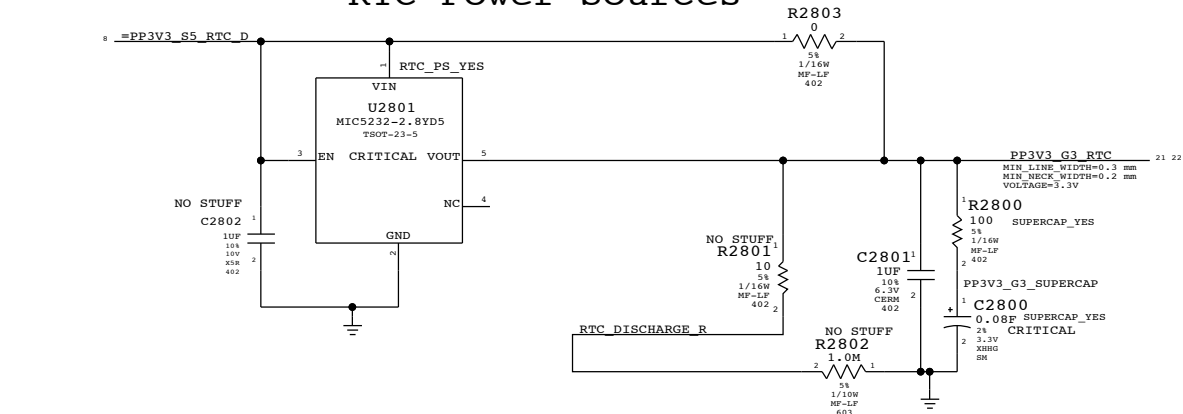
REV.: B

SCALE: NONE

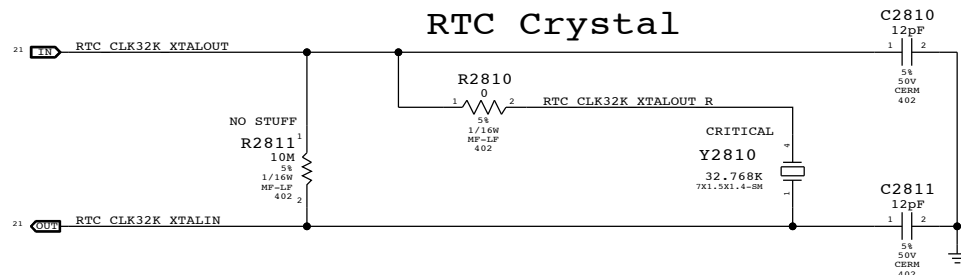
SBT: 24

OF: 98

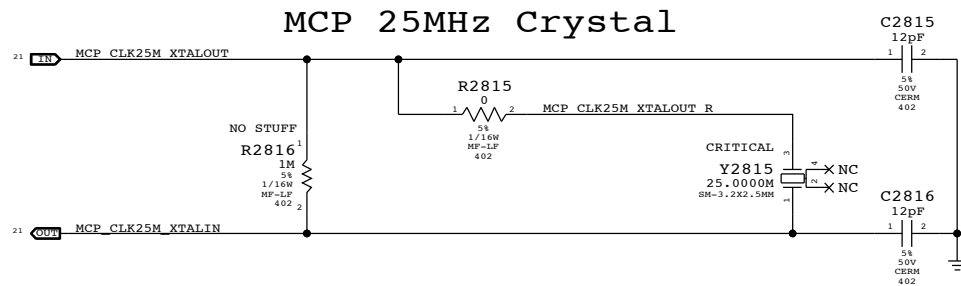
RTC Power Sources



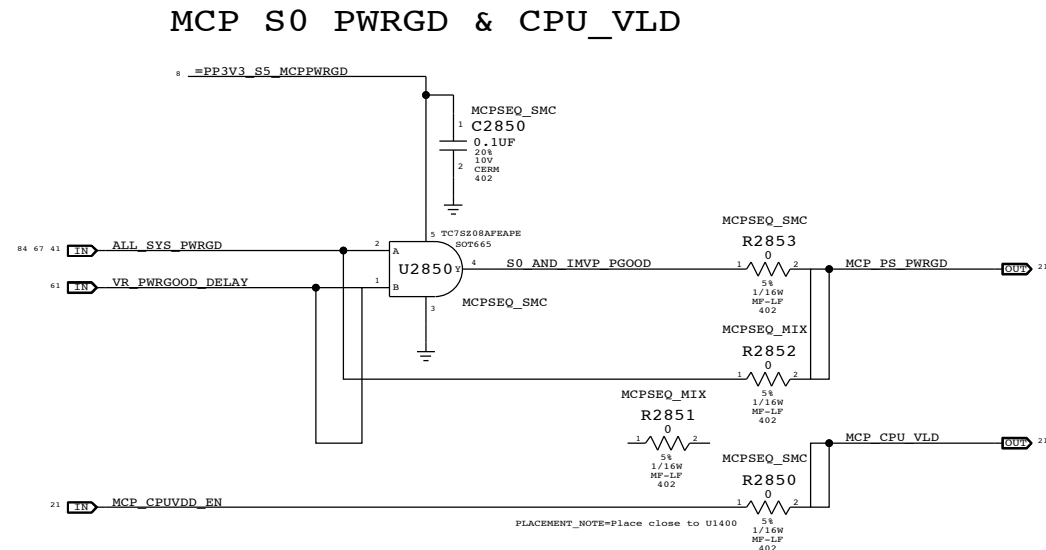
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

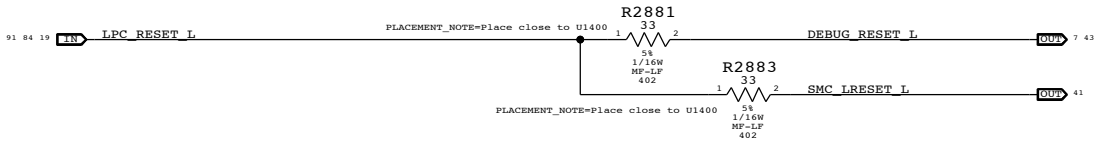
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

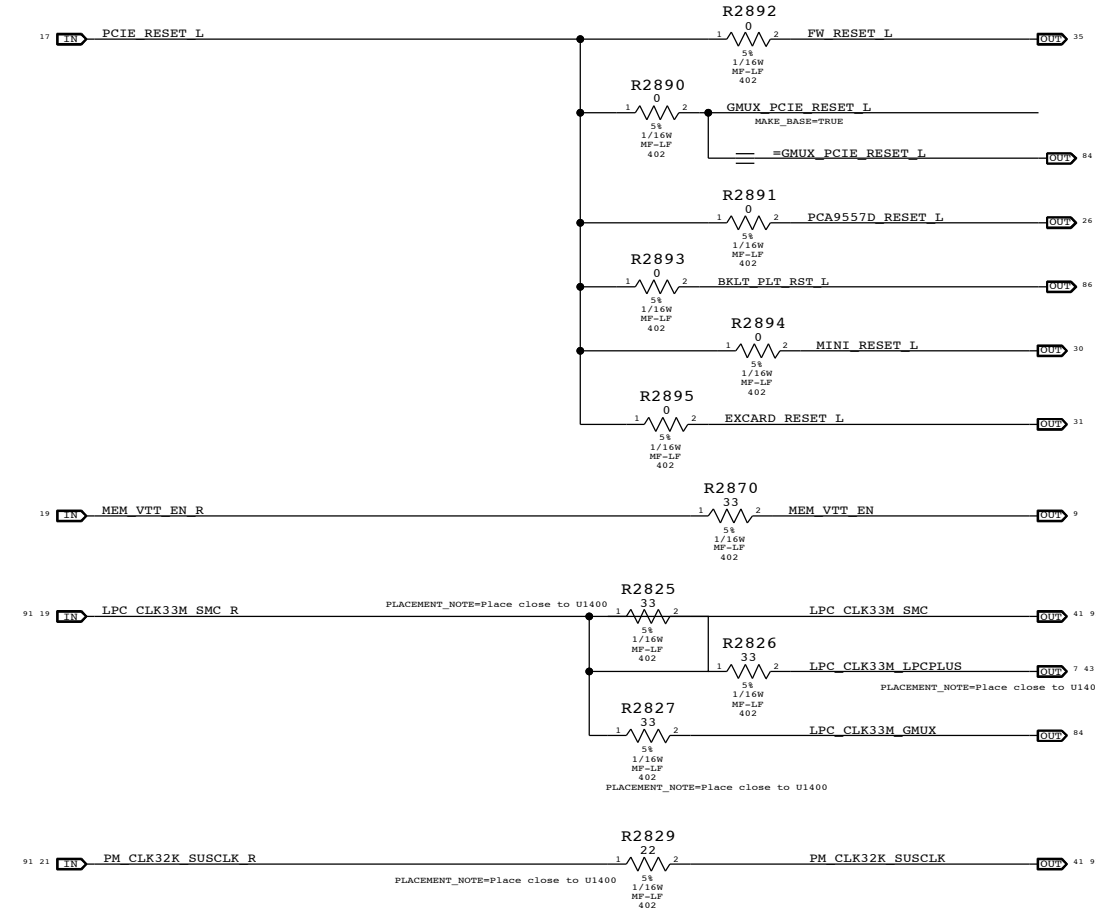
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

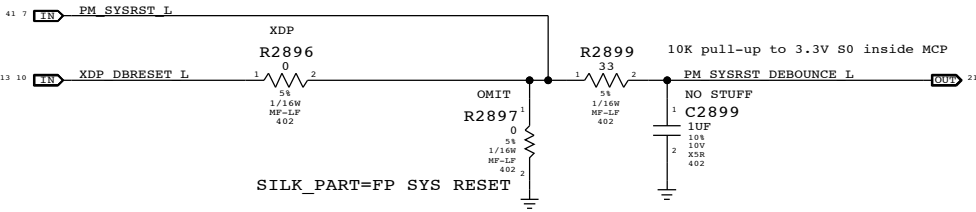
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc

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SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHR	OF
NONE	25	98

Page Notes

Power aliases required by this page:

- PP3V3_S3_VREFMRGN
- PP3V3_S5_VREFMRGN
- PPVTT_S3_DDR_BUF

Signal aliases required by this page:

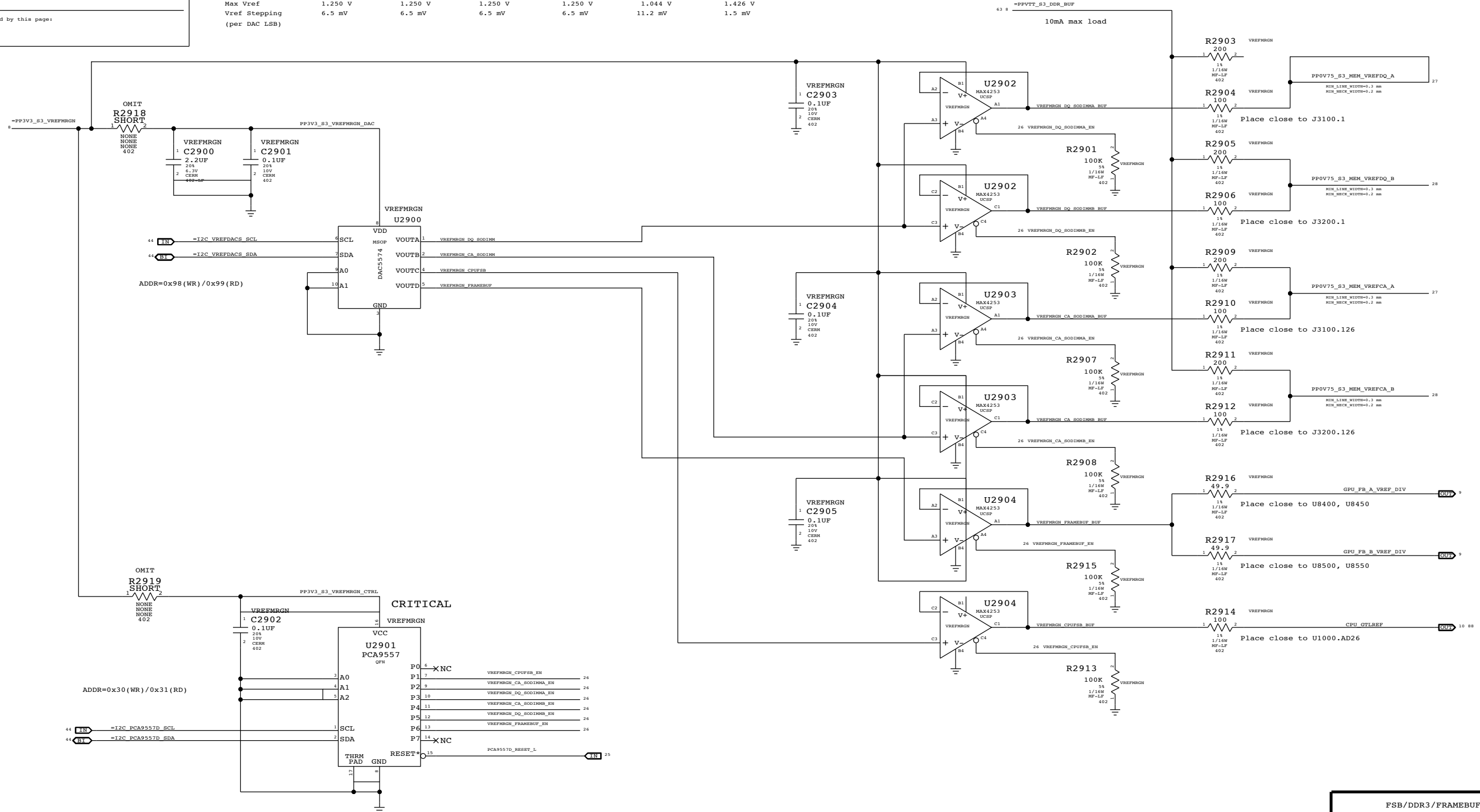
- T2C_VREFDAC_SCL
- T2C_VREFDAC_SDA
- T2C_PCA9557D_SCL
- T2C_PCA9557D_SDA

BOM options provided by this page:

VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ		MEM A VREF CA		MEM B VREF DQ		MEM B VREF CA		CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	A	B	C	D		
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00		
Max DAC code	0x87	0x87	0x87	0x87	0x87	0x87	0x55	0xFF		
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA		
Max source I	5 mA	5 mA	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA		
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V		
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V		
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V		
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV		

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

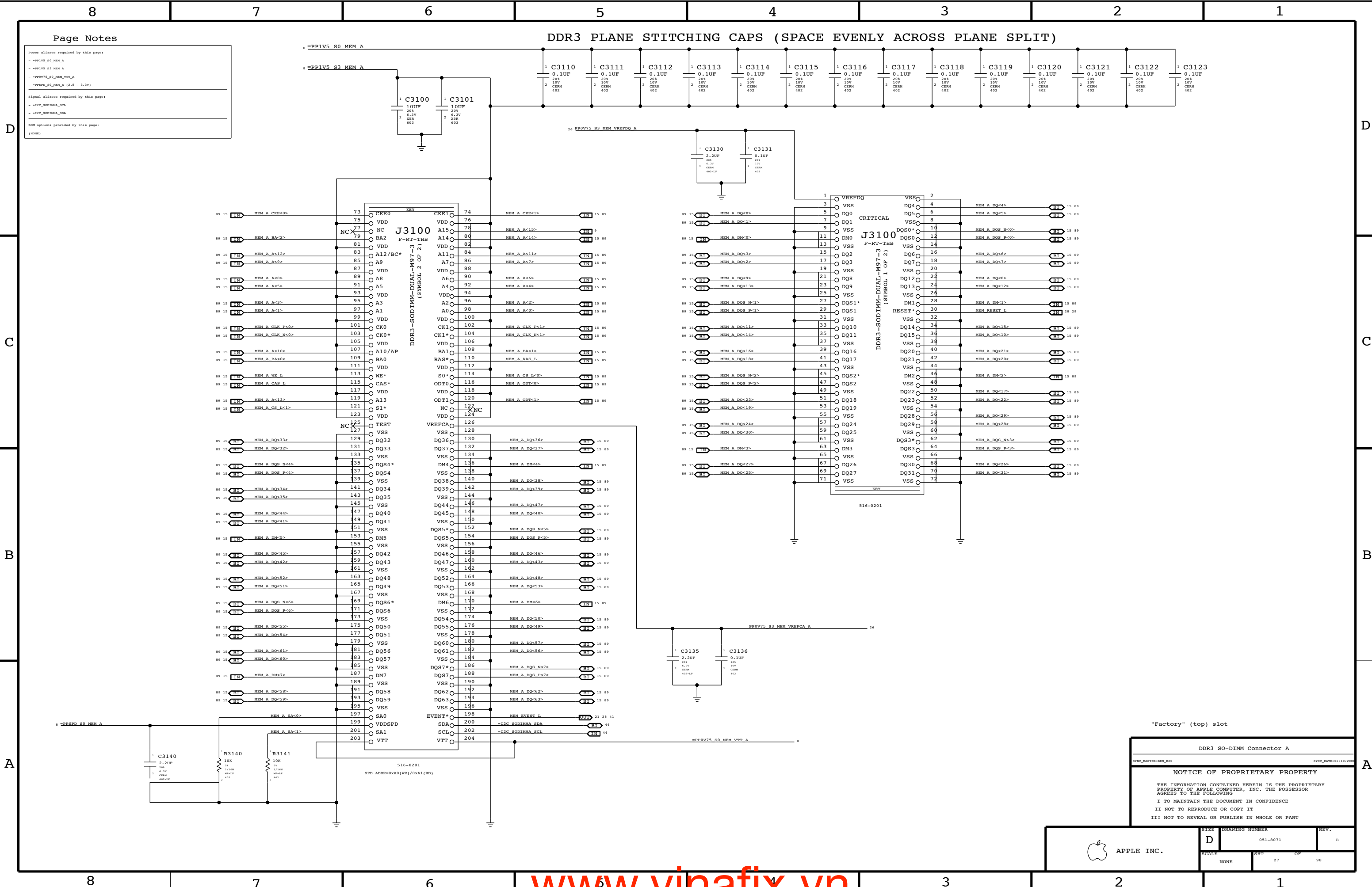
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SCALE	SCALE	SCALE	SCALE
NONE	26	OF	98



Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

DEM options provided by this page:

(NONE)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=MEM_R20 SYNC_DATE=06/10/2008

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D

SCALE NONE

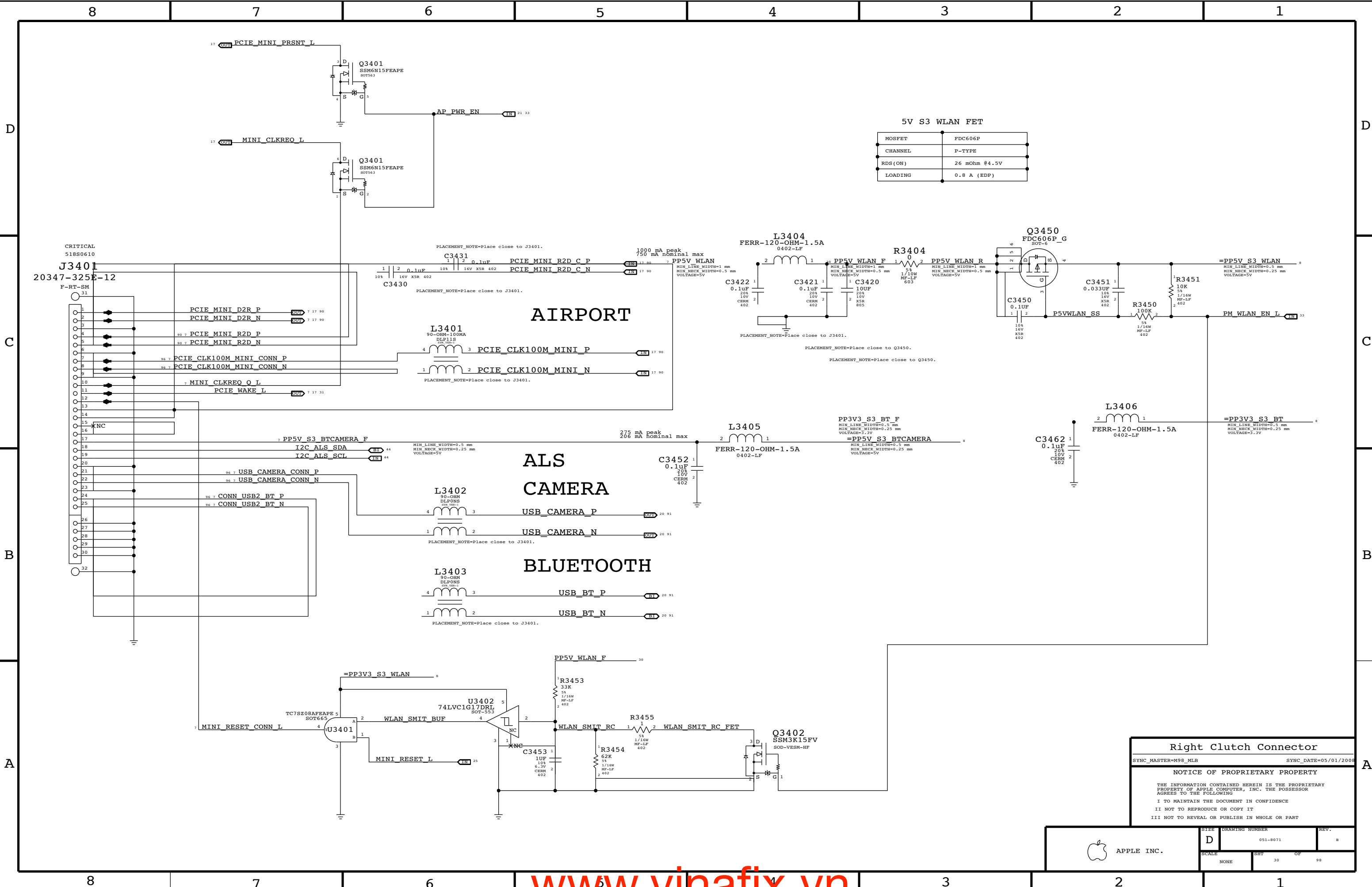
SIZE DRAWING NUMBER 051-8071

REV. B

27 OF 98

www.vinafix.vn





5V S3 WLAN FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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SCALE: NONE SBT: 30 OF: 98

REV. B

EXPRESSCARD/34 FLEX CONNECTOR

D

D

C

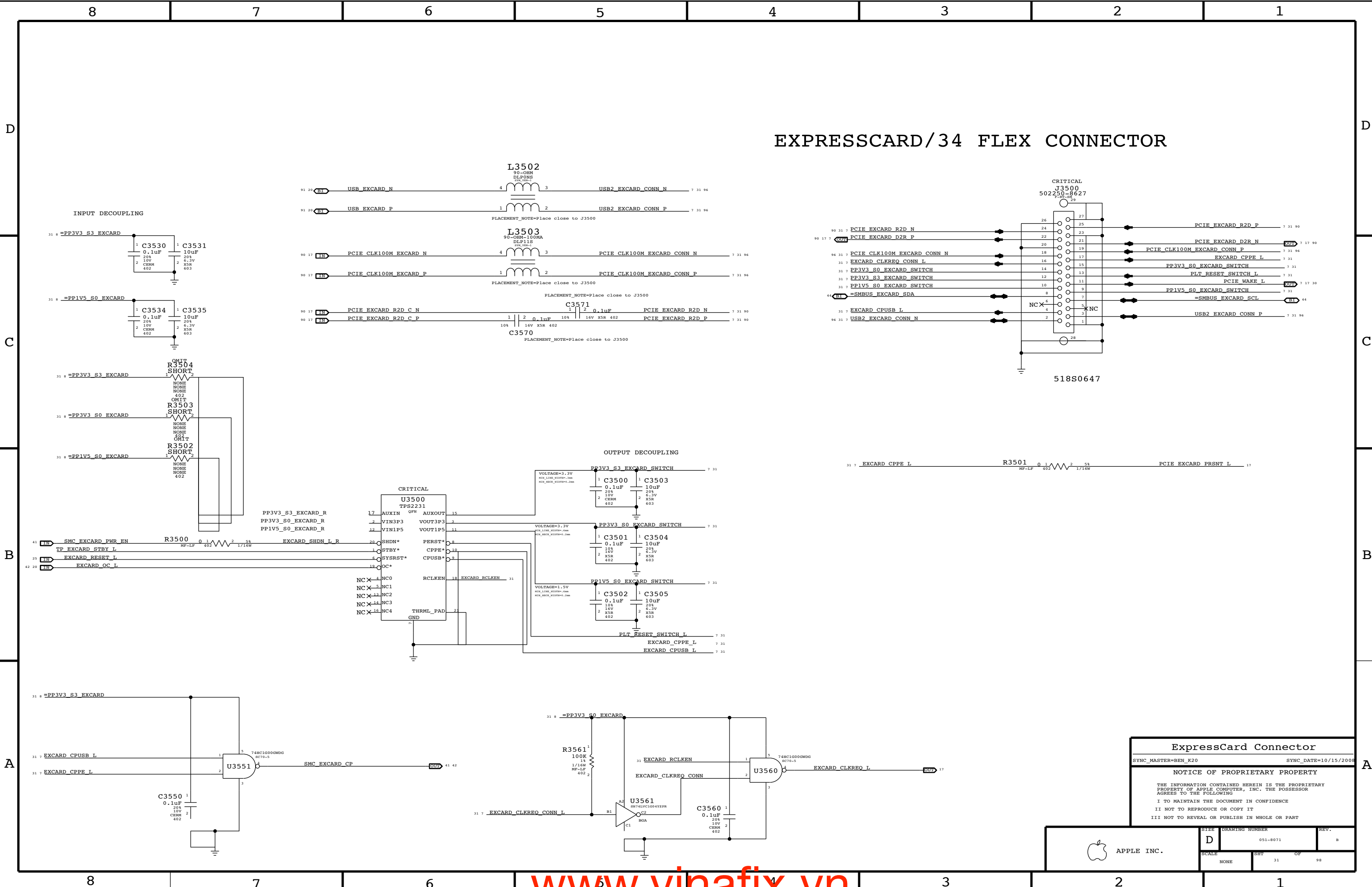
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ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

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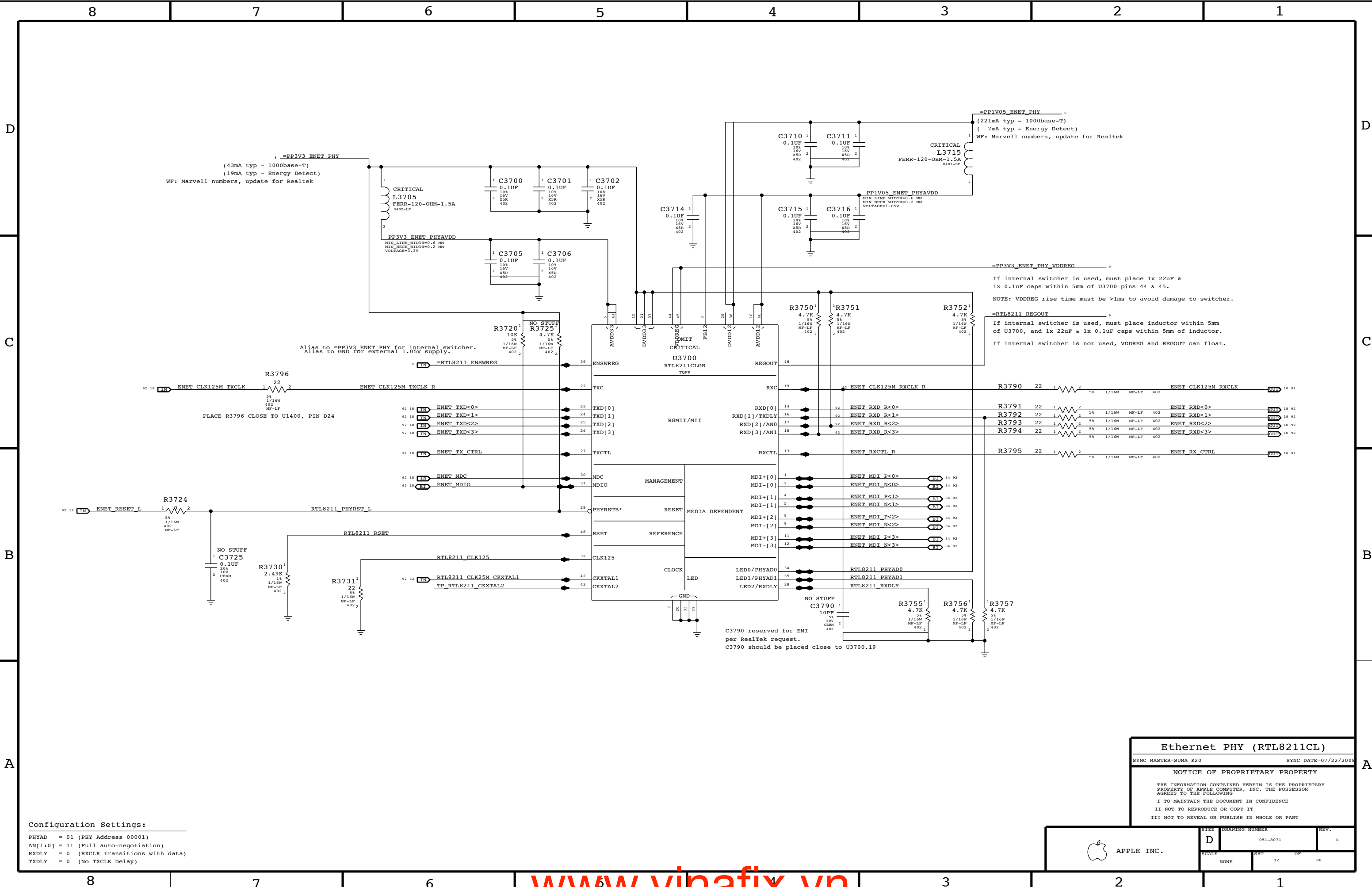
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE: D DRAWING NUMBER: 051-8071 REV: B

SCALE: NONE SBT: 31 OF: 98



Configuration Settings:

PHYAD	= 01 (PHY Address 00001)
AN[1:0]	= 11 (Full auto-negotiation)
RXDLY	= 0 (RXCLK transitions with data)
TXDLY	= 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20

SYNC_DATE=07/22/2008

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SCALE

NONE

SIZE

D

DRAWING NUMBER

051-8071

REV.

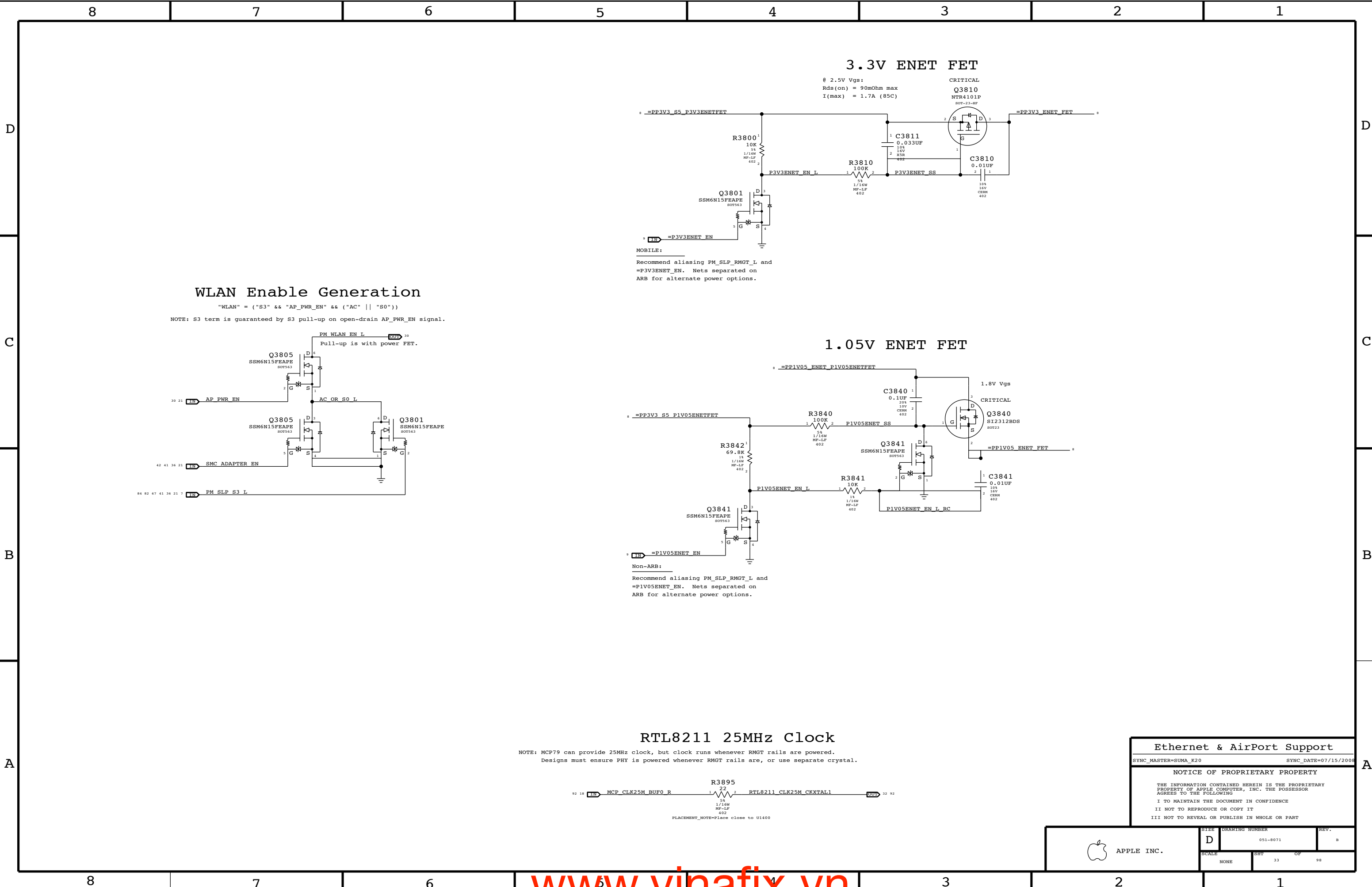
B

SHEET

32

OF

98

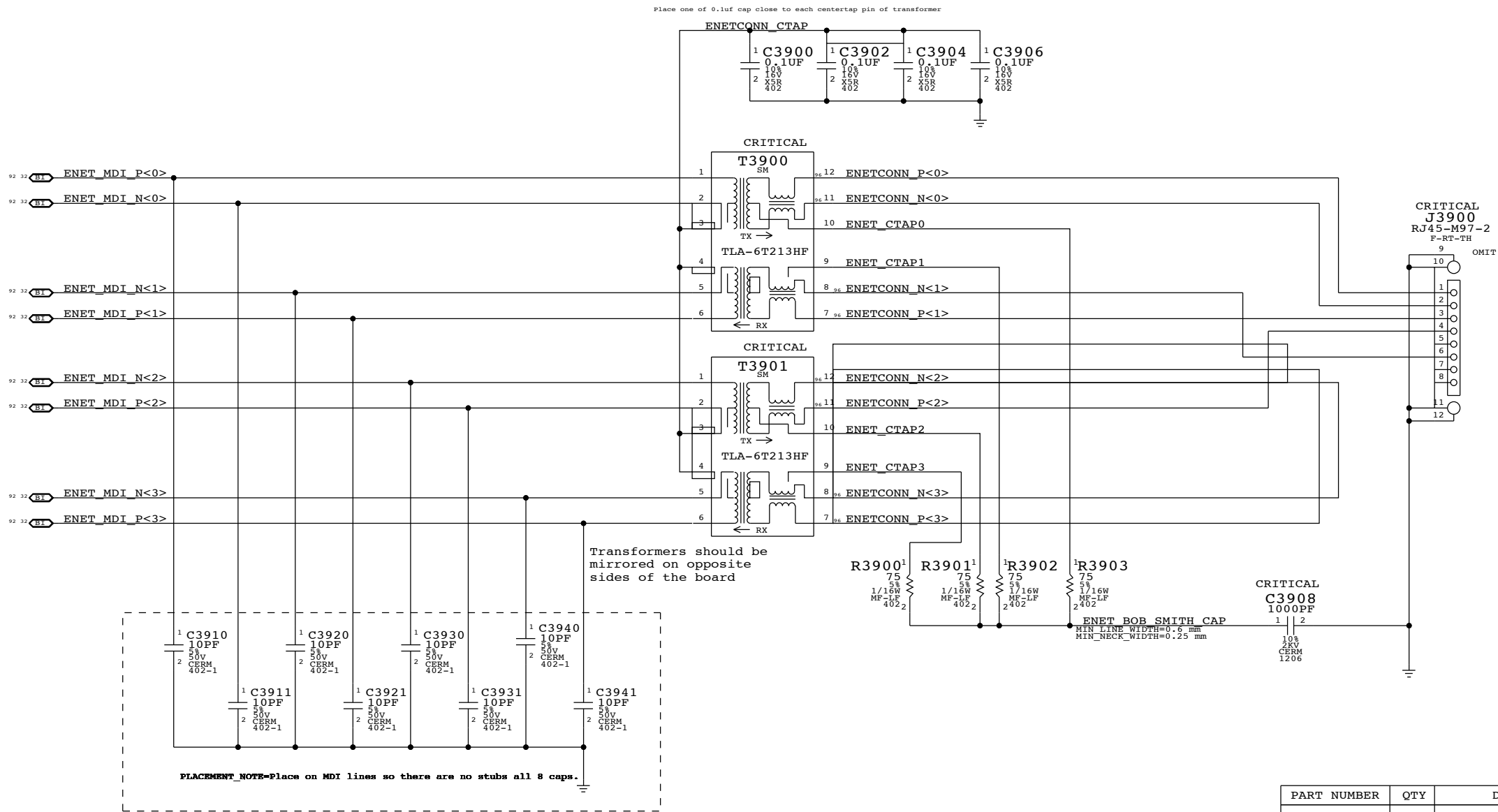


Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN, RJ45, HB, 10/100TX	J3900	CRITICAL	

Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

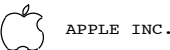
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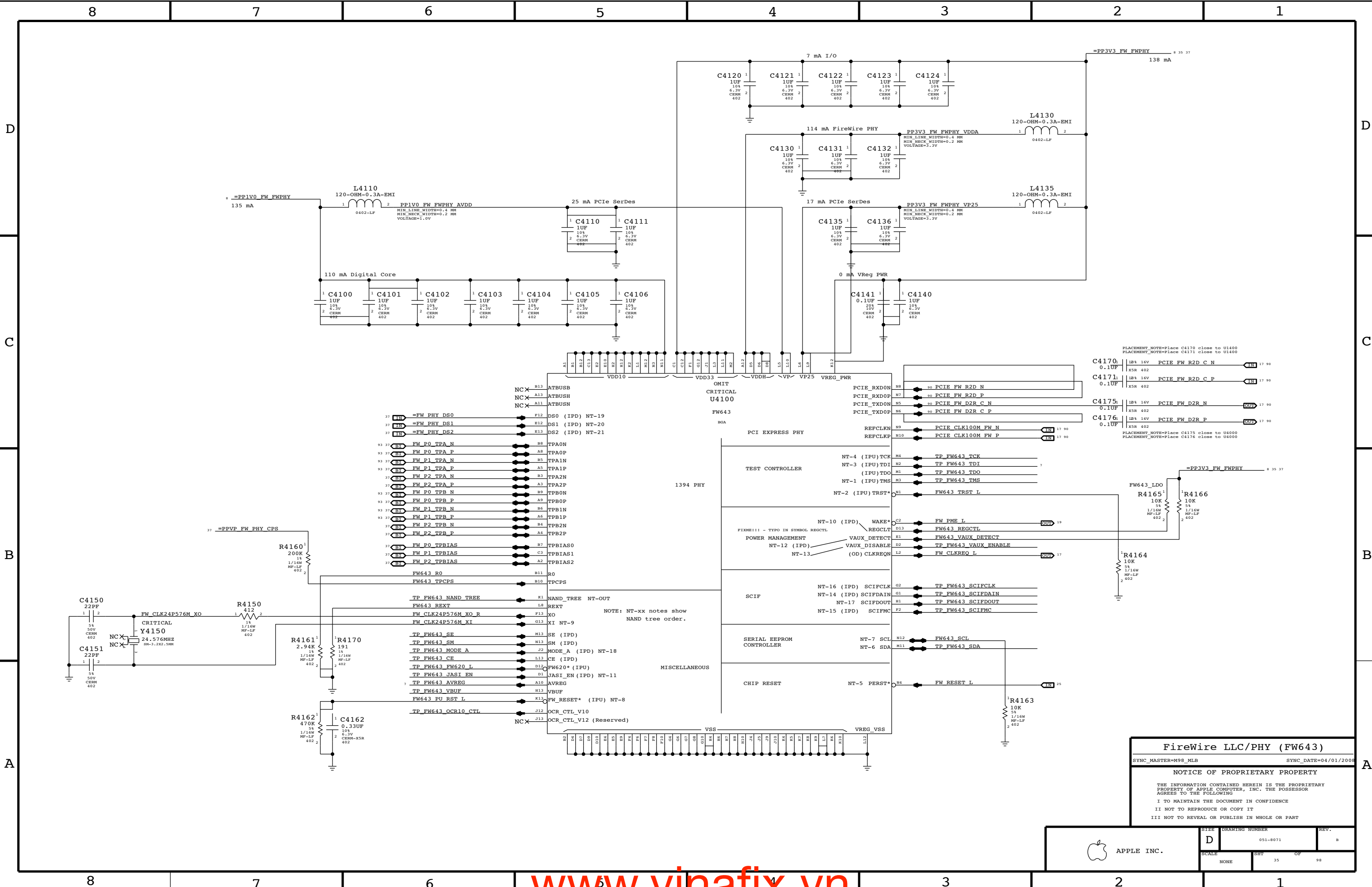


APPLE INC.

SIZE: DRAWING NUMBER REV.

D 051-8071 B

SCALE SBT OF 98



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008


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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SHT	OF
NONE	35	98

Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

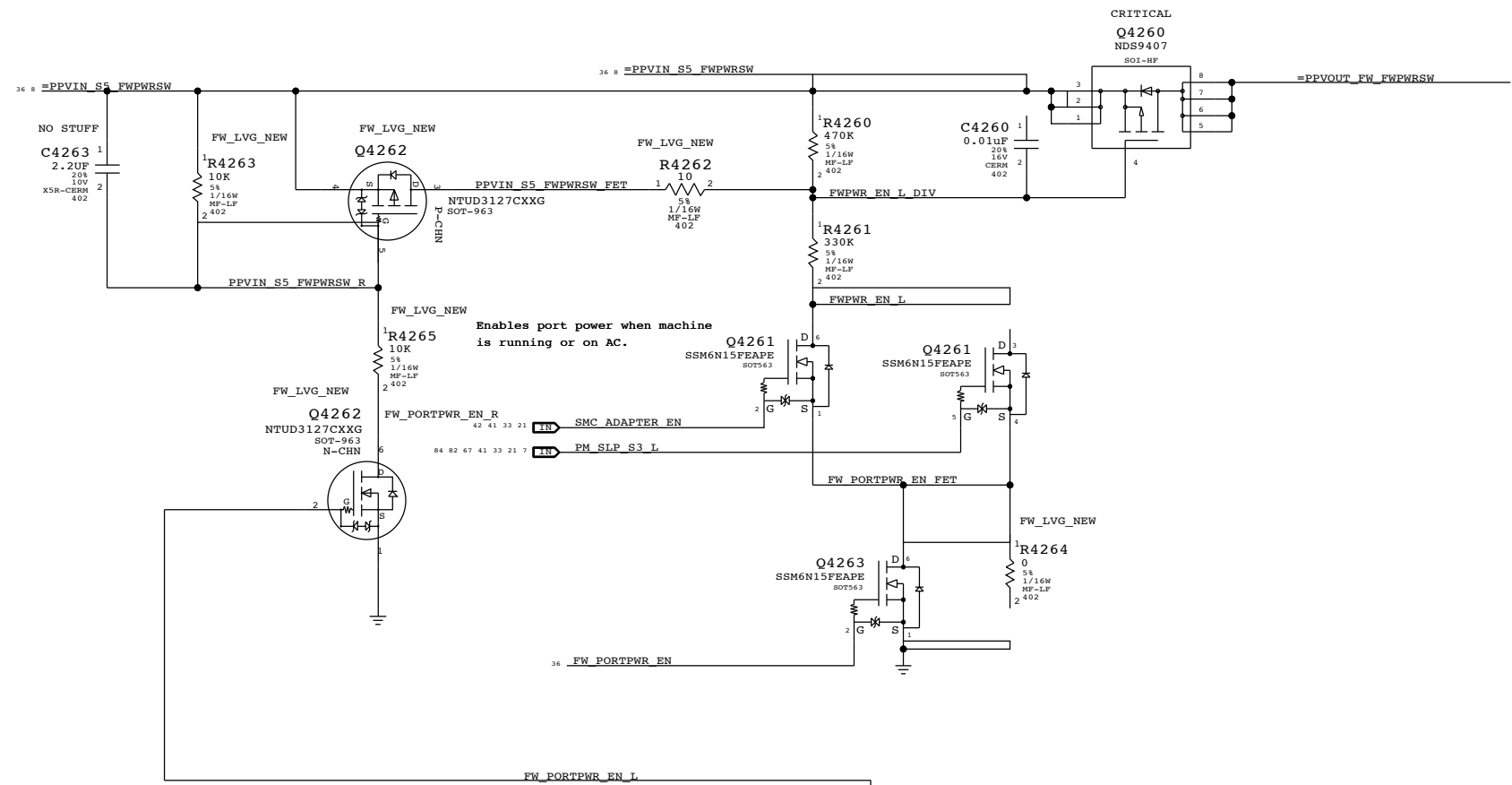
Signal aliases required by this page:

(NONE)

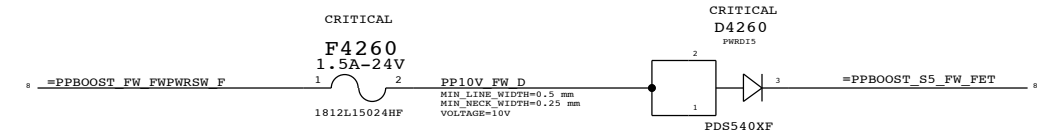
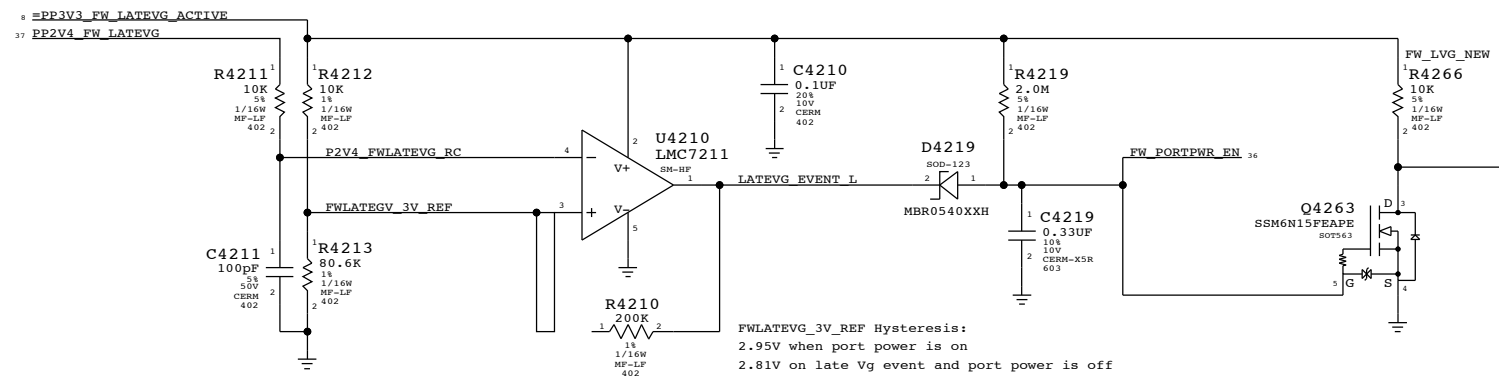
BOM options provided by this page:

- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

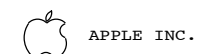
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SIZE: DRAWING NUMBER: REV.

D 051-8071 B

SCALE: NONE SBT 36 OF 98

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)

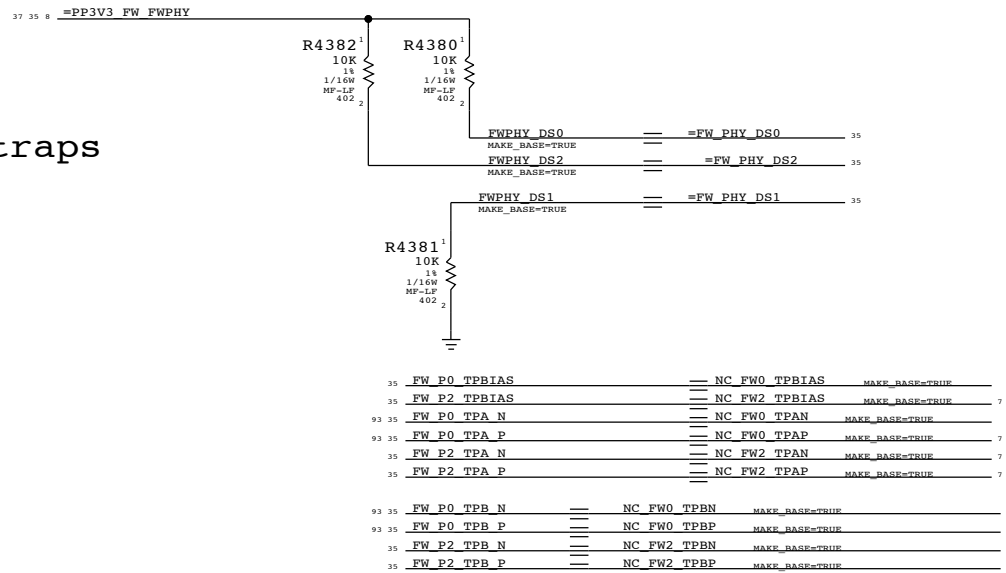
NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

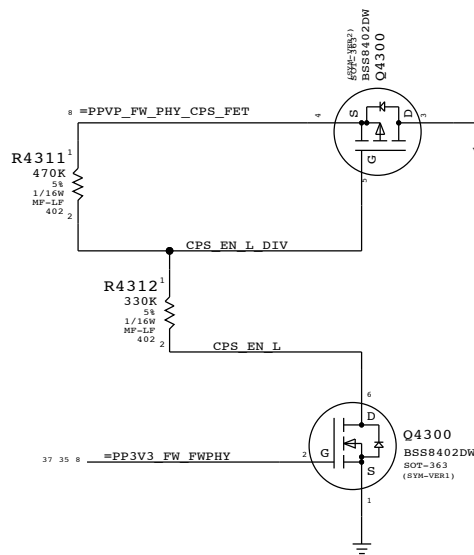
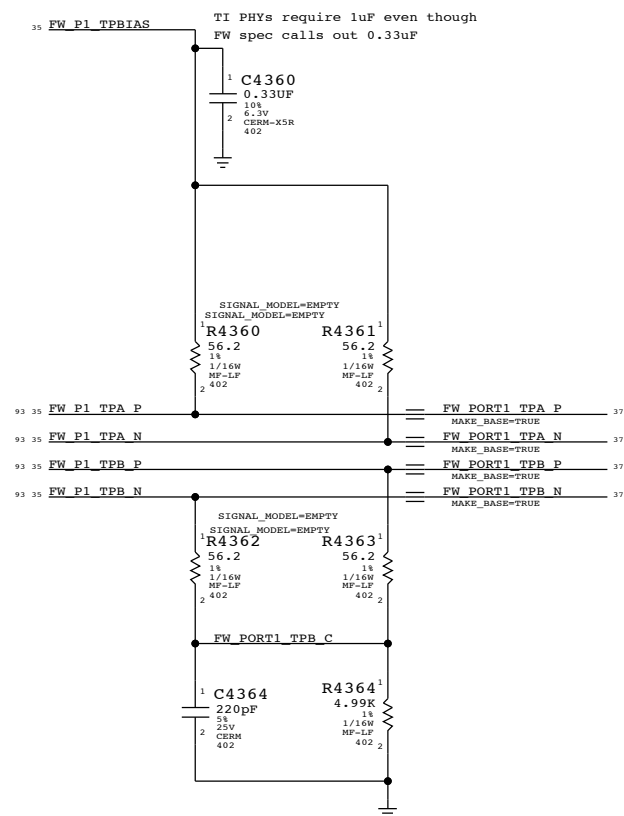
Configures PHY for:

- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

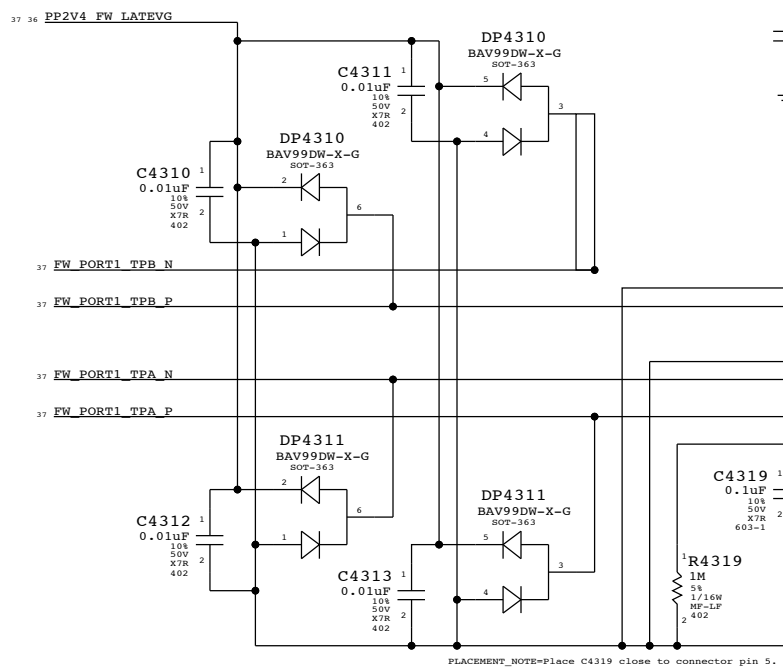


Termination

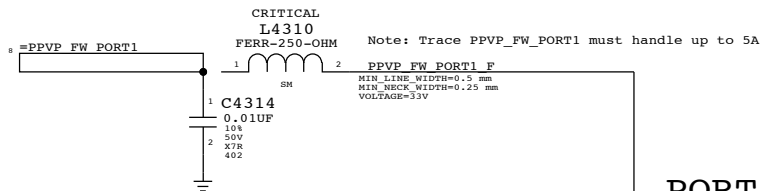
Place close to FireWire PHY



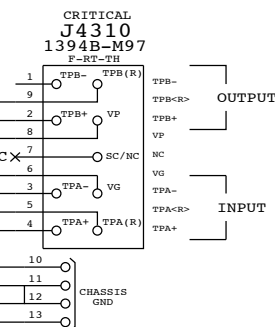
"Snapback" & "Late VG" Protection



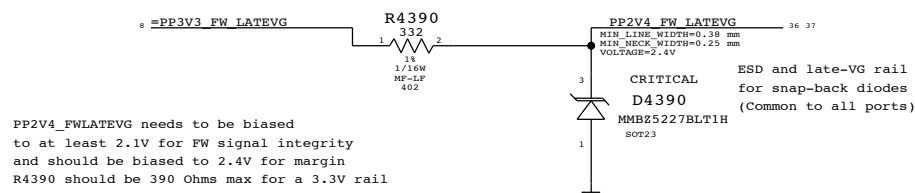
Cable Power



PORT 1 BILINGUAL



Late-VG Protection Power



FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

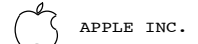
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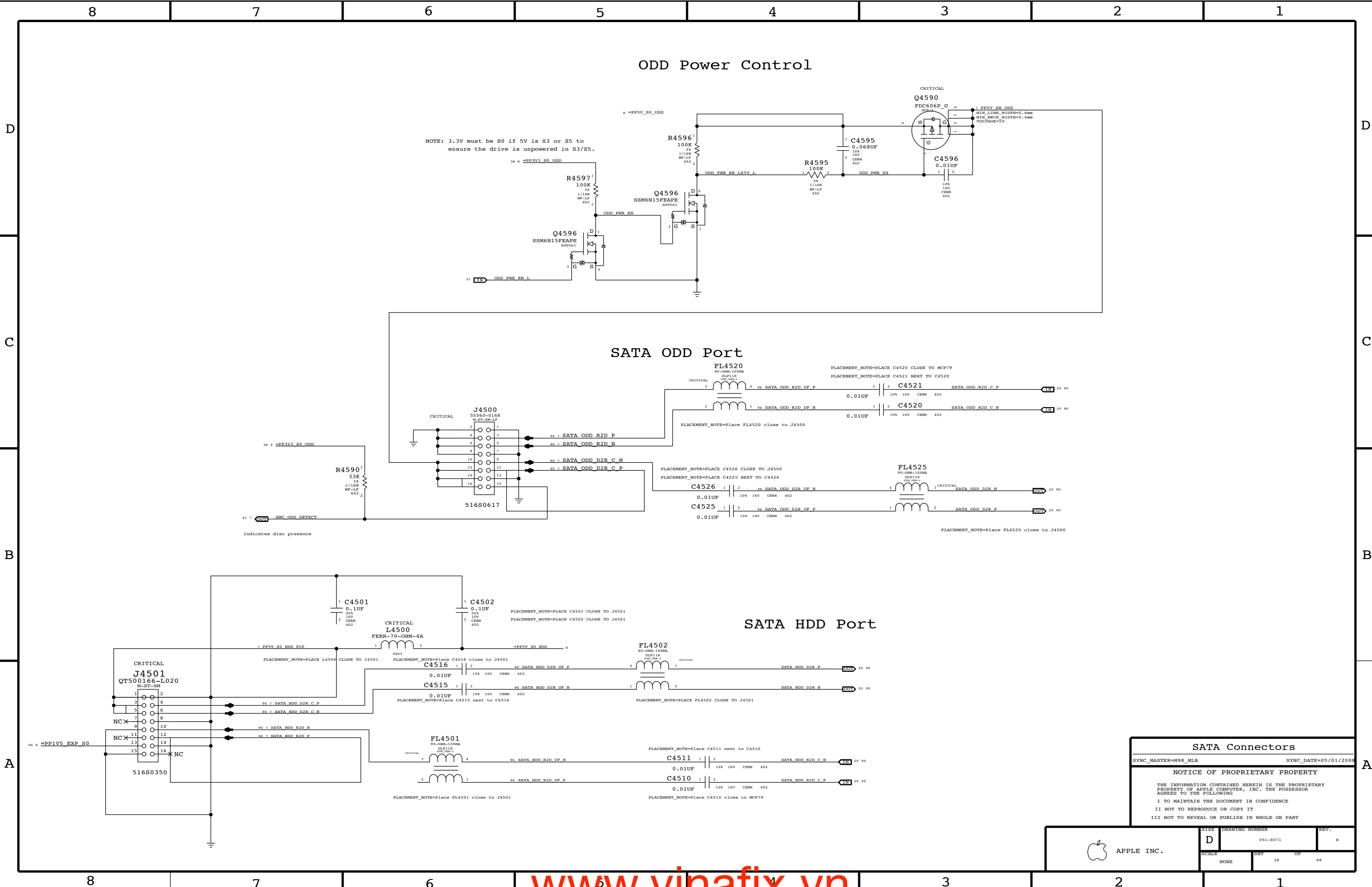
II NOT TO REPRODUCE OR COPY IT

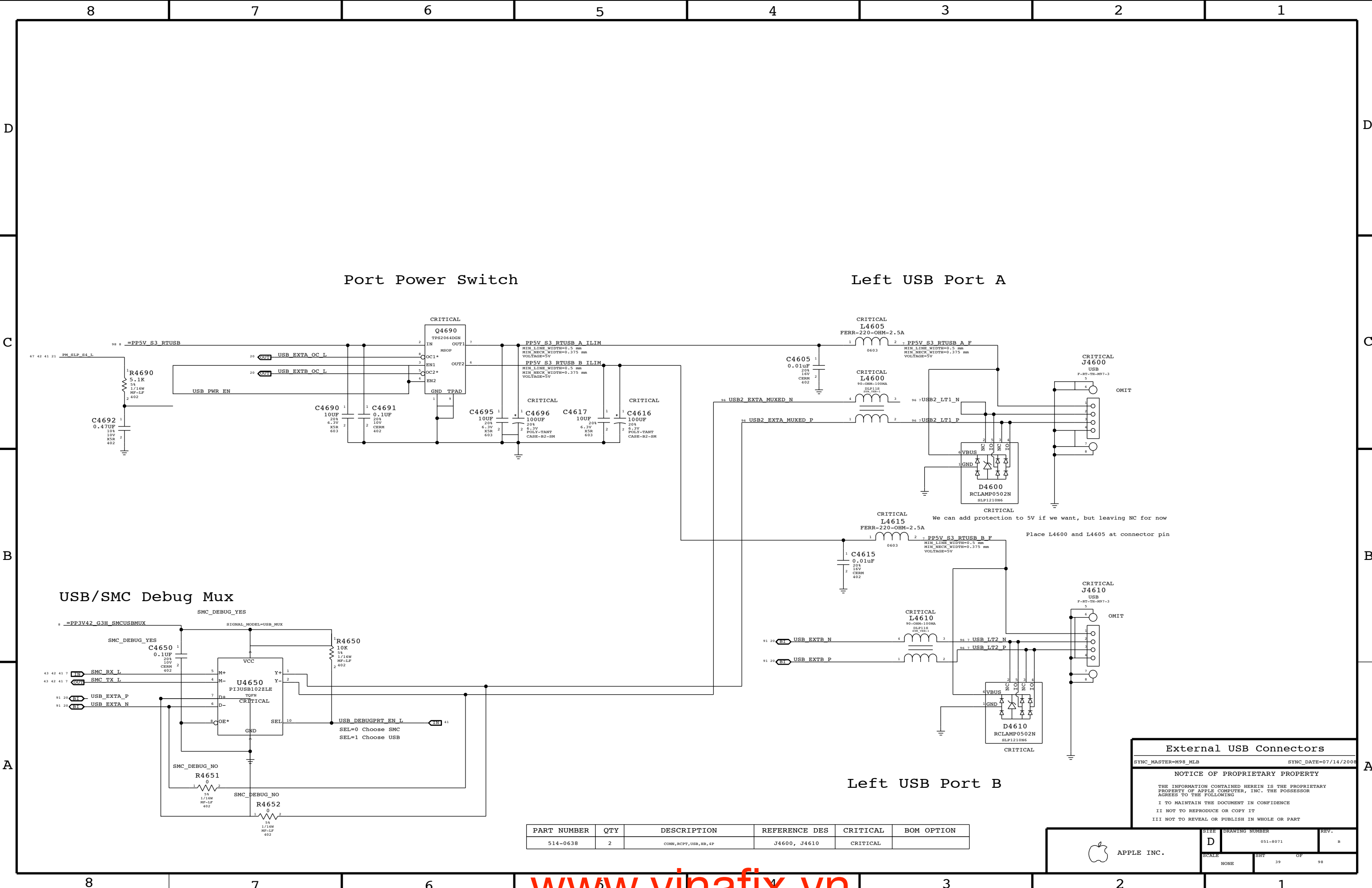
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



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SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SBT	OF
NONE	37	98





Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

External USB Connectors

SYNC_MASTER=M98_MLB

SYNC_DATE=07/14/2008

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN, RCPT, USB, HB, 4P	J4600, J4610	CRITICAL	

APPLE INC.

SIZE

D

DRAWING NUMBER

051-8071

REV.

B

SCALE

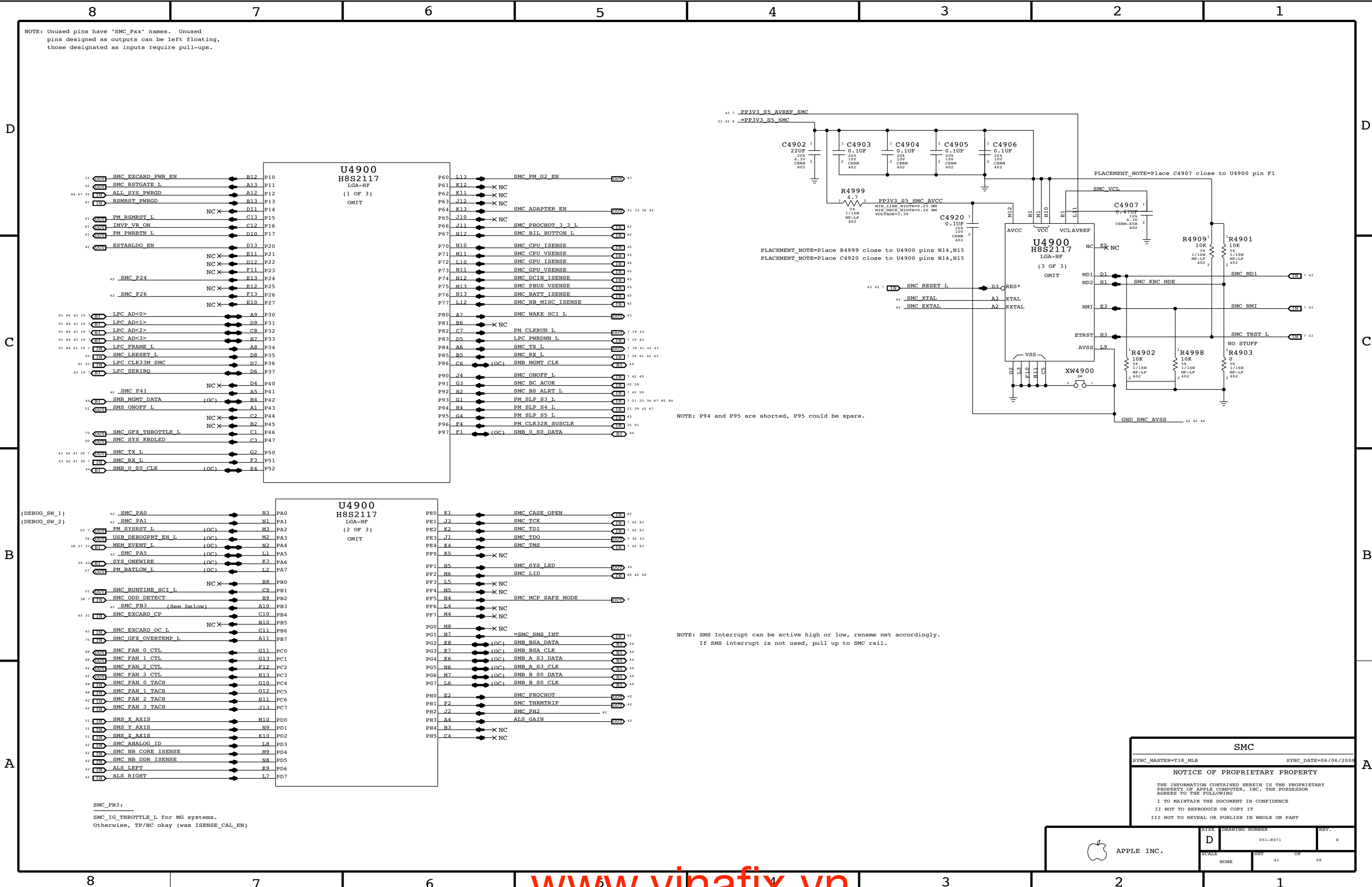
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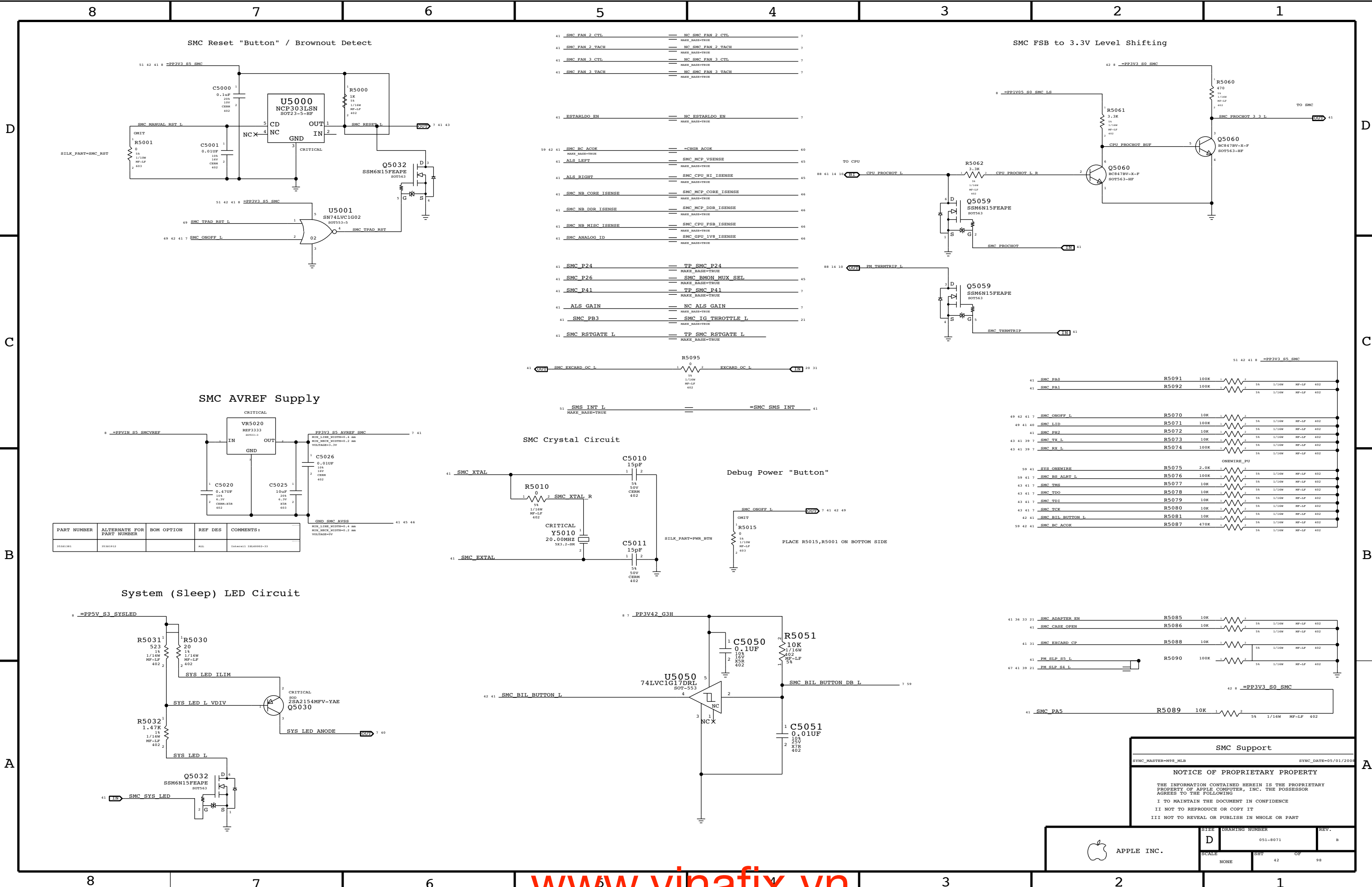
SHT

39

OF

98





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381912		ALL	Interval1 SR6000-33

SMC Support

SYNC_MASTER=M98_NLB SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

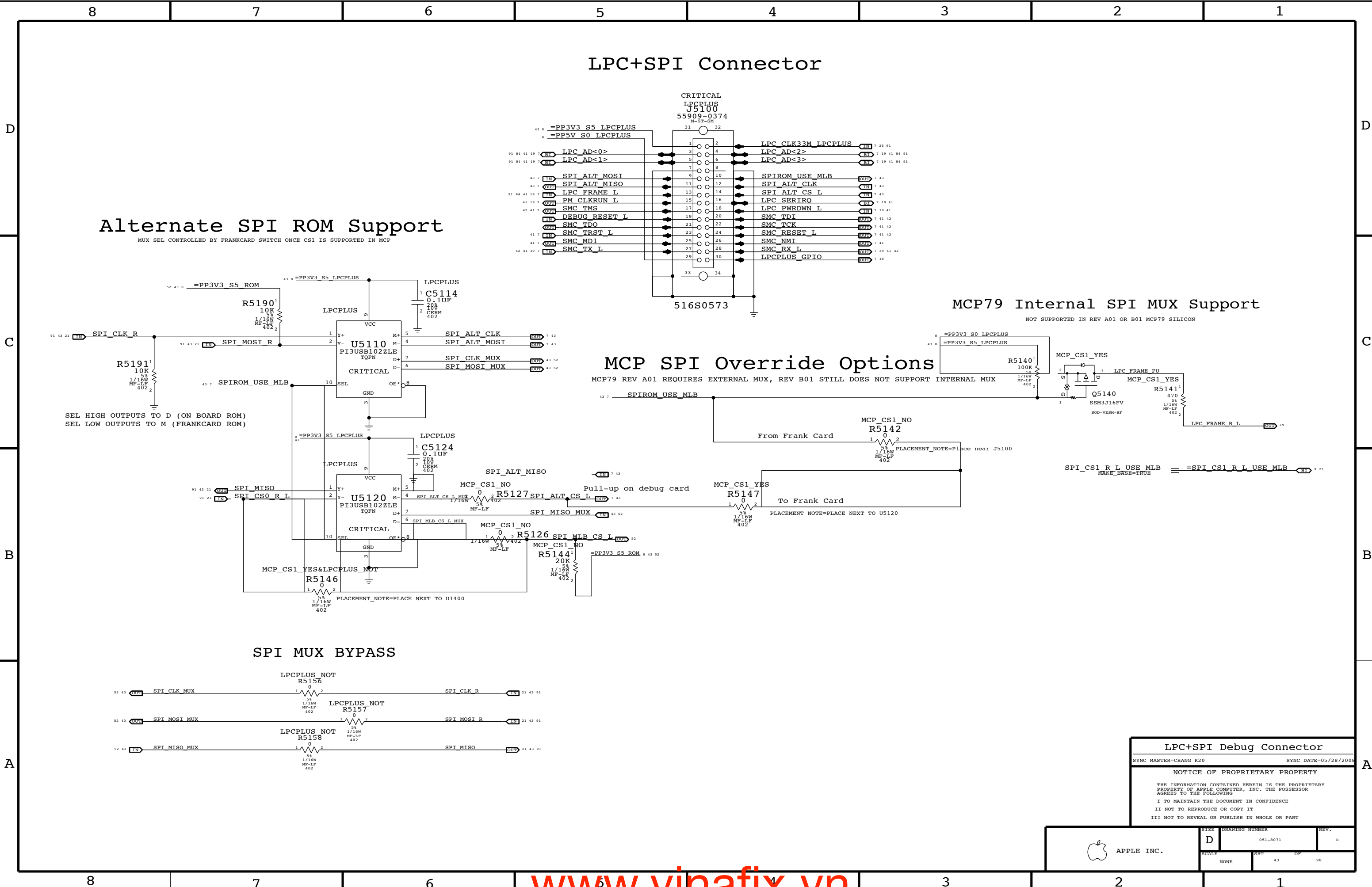
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	D	051-8071	B
SCALE	NONE	SBT	OF
	42	98	



LPC+SPI Connector

Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

SPI MUX BYPASS

LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

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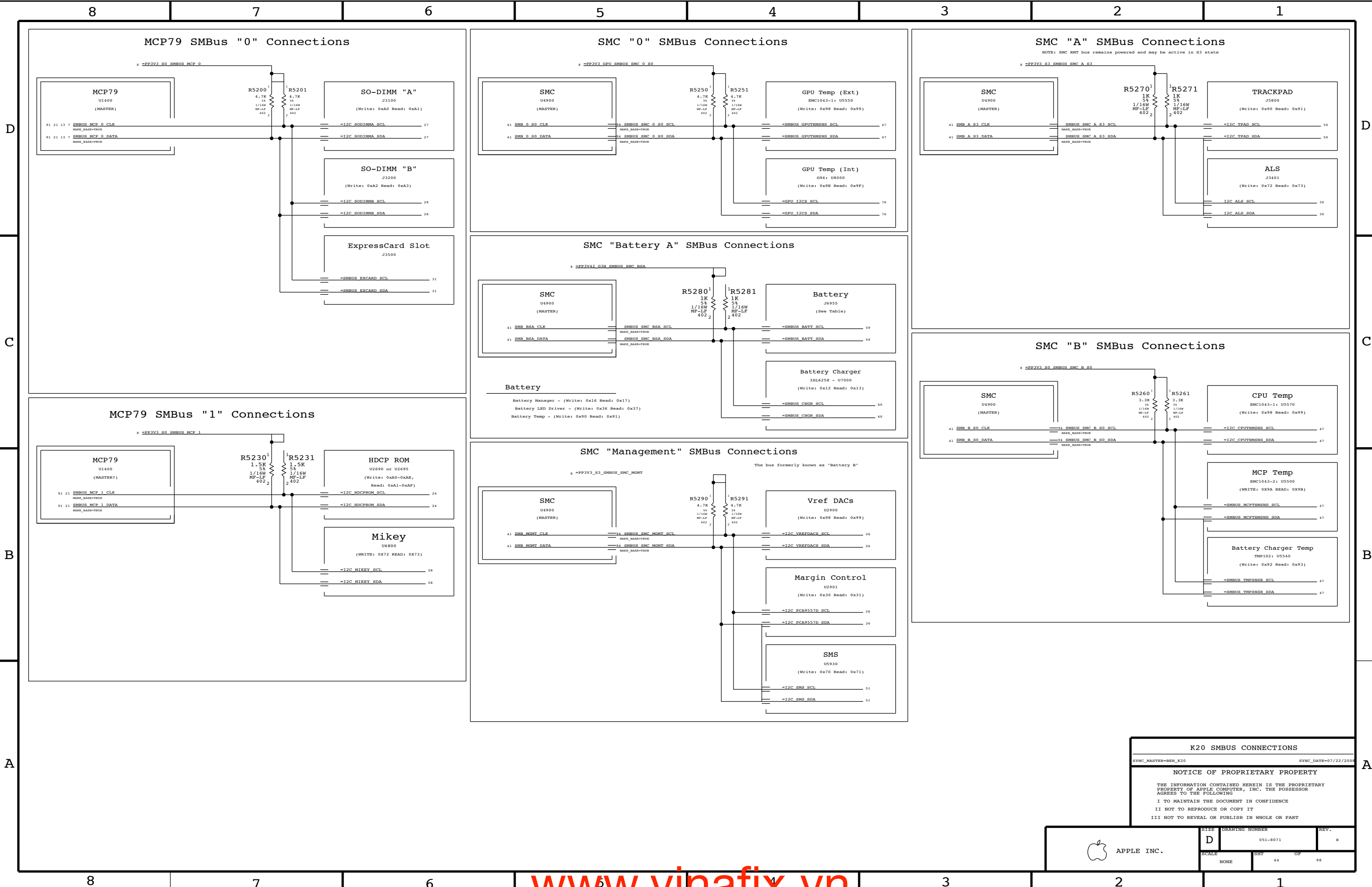


APPLE INC.

SIZE: DRAWING NUMBER REV.

D 051-8071 B

SCALE: NONE SBT 43 OF 98



K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

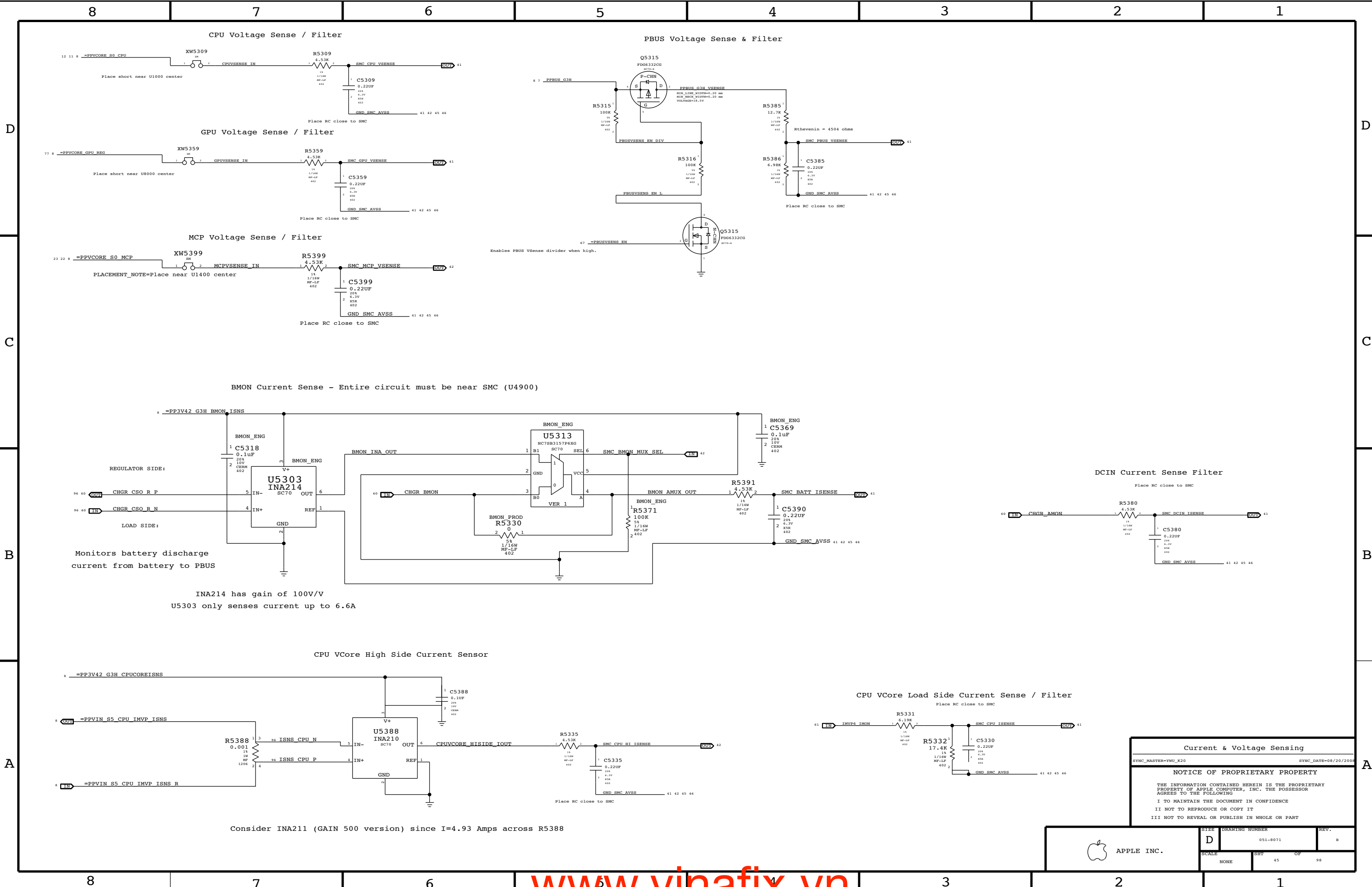
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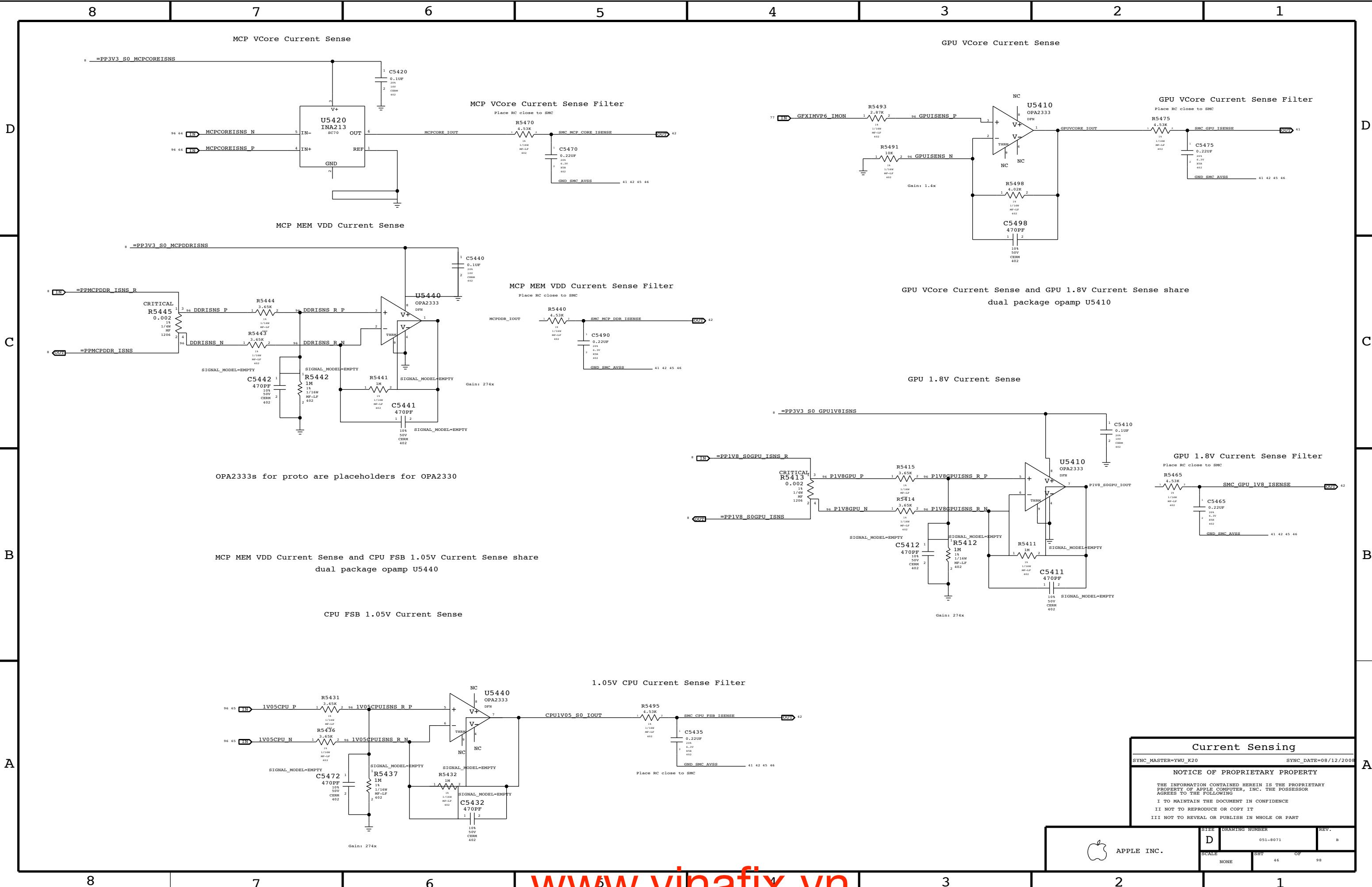
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OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

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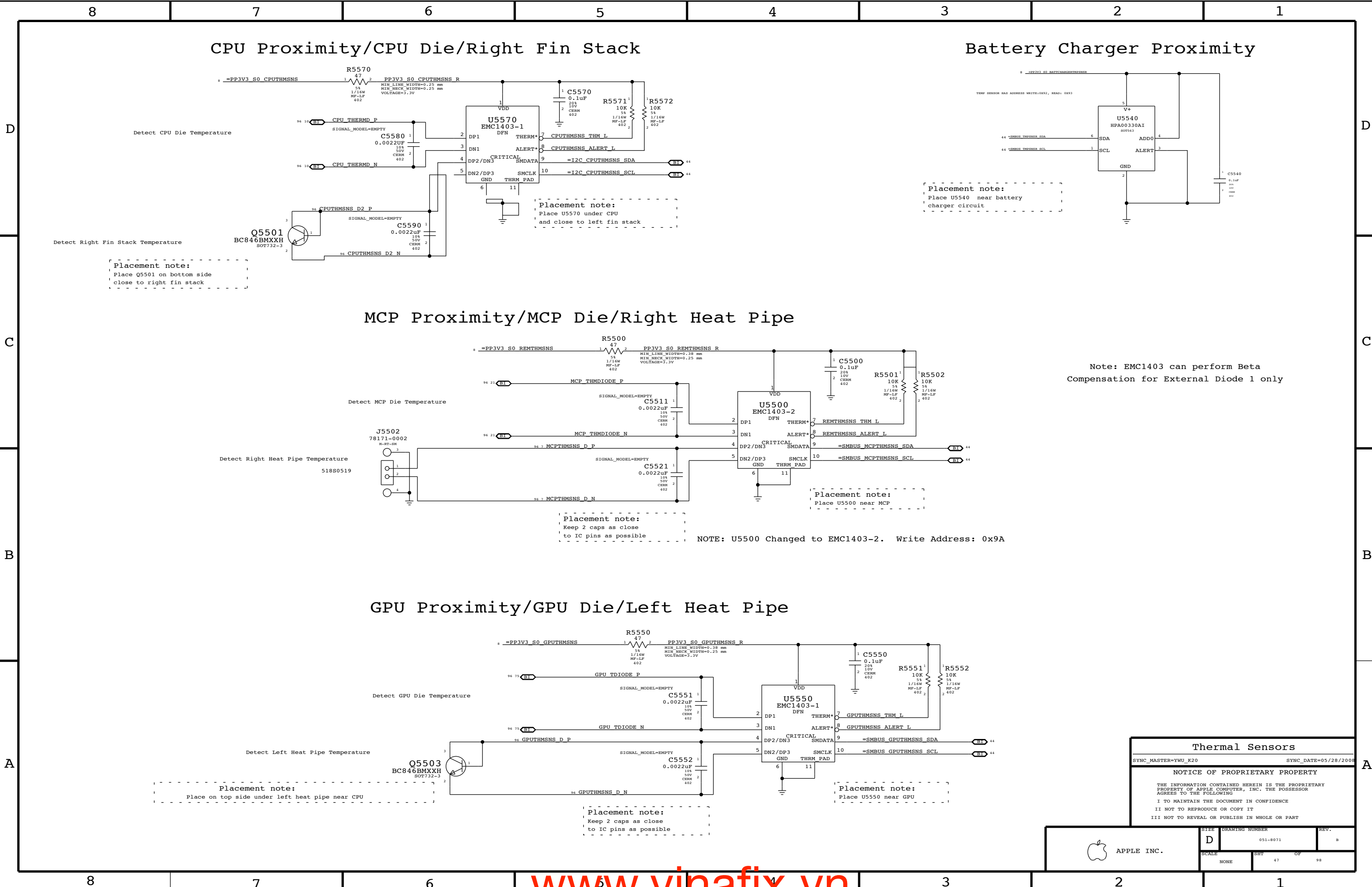
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	D	051-8071	
SCALE		SH	OF
NONE		46	98



CPU Proximity/CPU Die/Right Fin Stack

Battery Charger Proximity

MCP Proximity/MCP Die/Right Heat Pipe

GPU Proximity/GPU Die/Left Heat Pipe

Thermal Sensors

SYNC_MASTER=YWU_K20

SYNC_DATE=05/28/2008


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SIZE: D

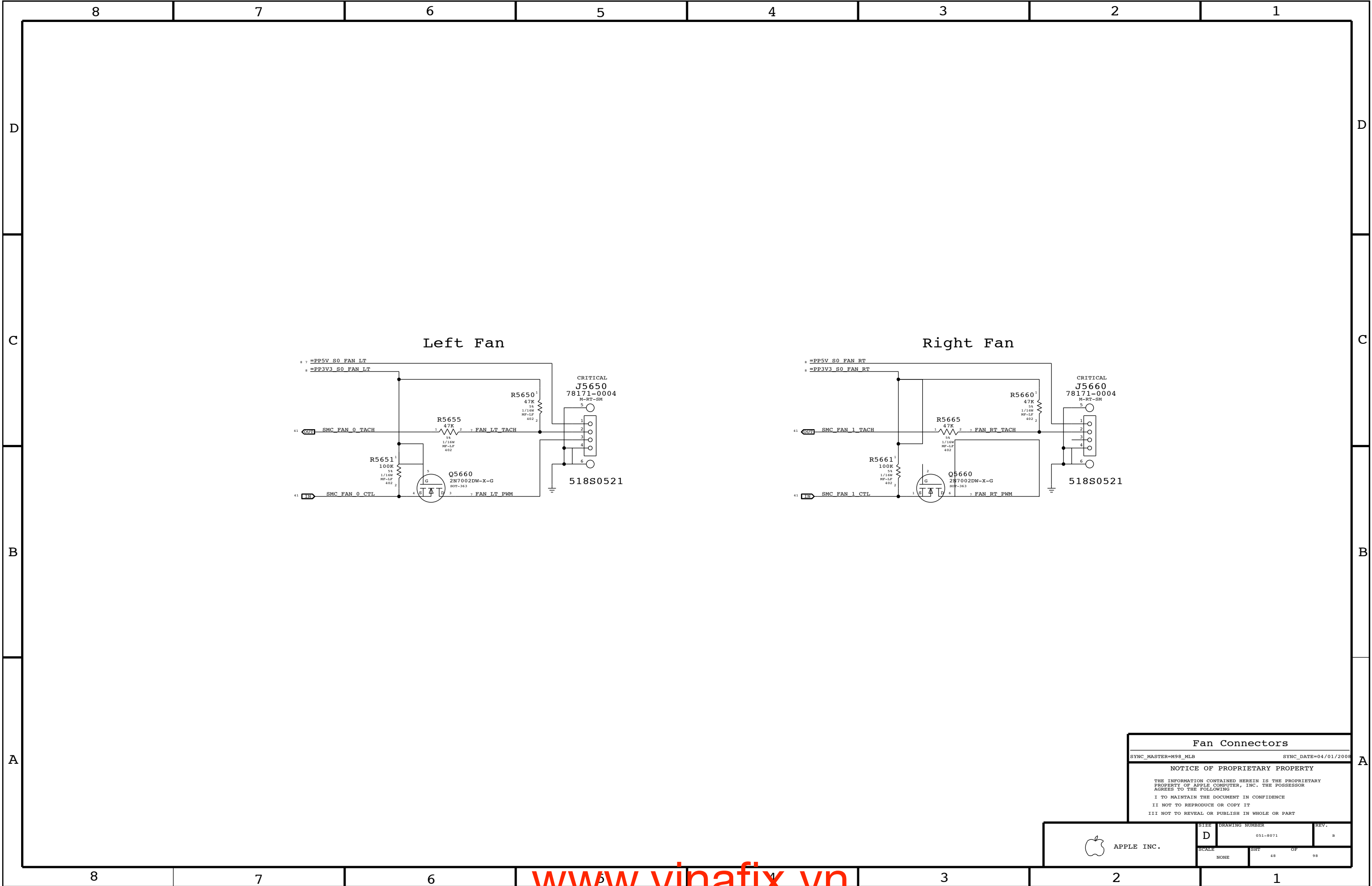
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REV.: B

SCALE: NONE

SBT: 47

OF: 98



D

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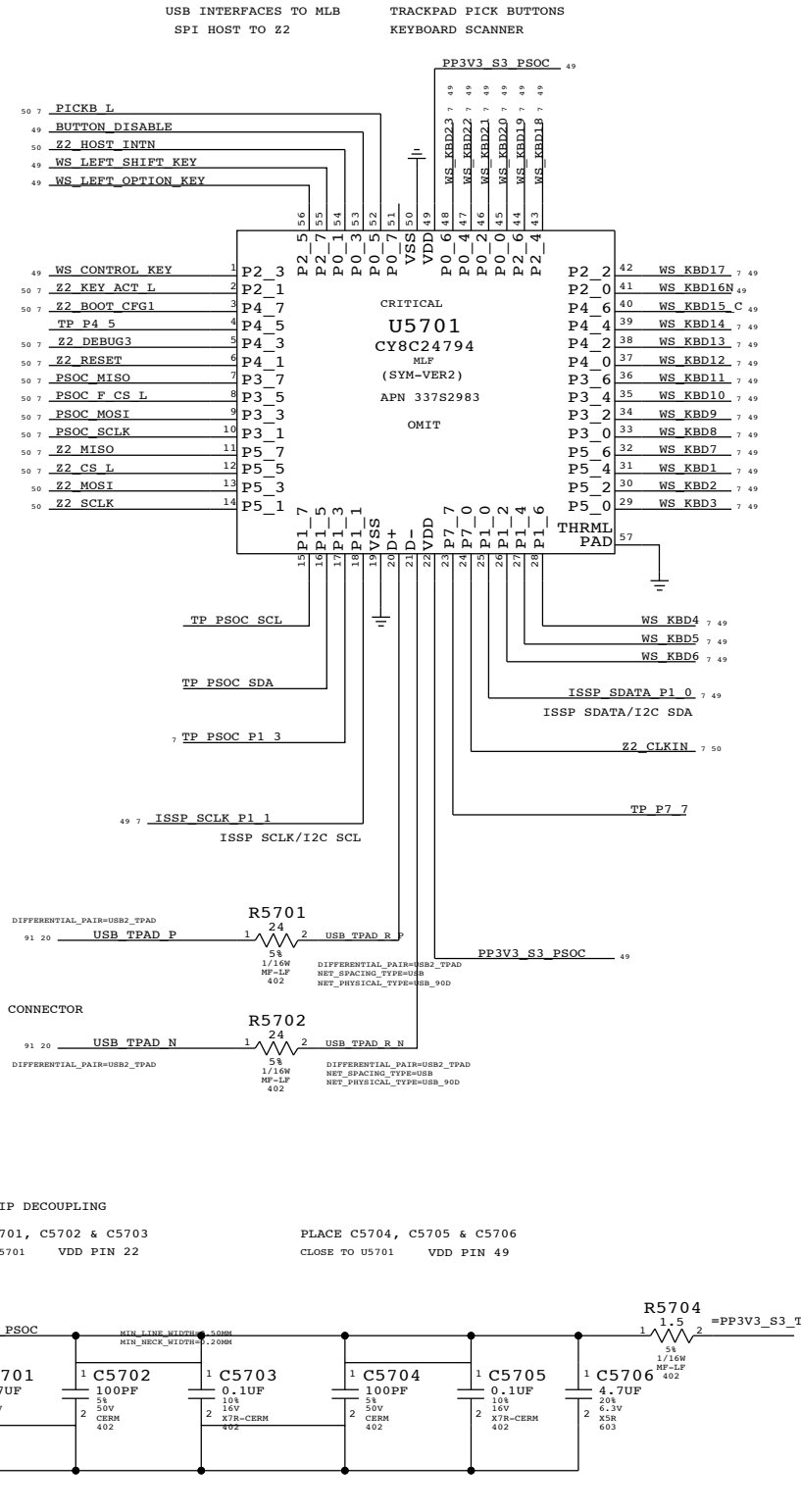
D

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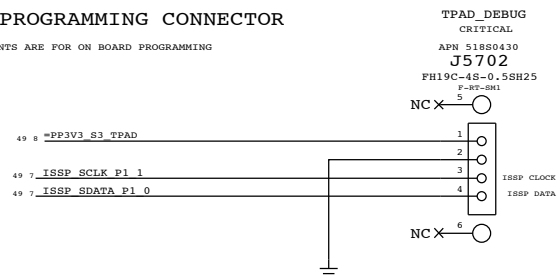
PSOC USB CONTROLLER



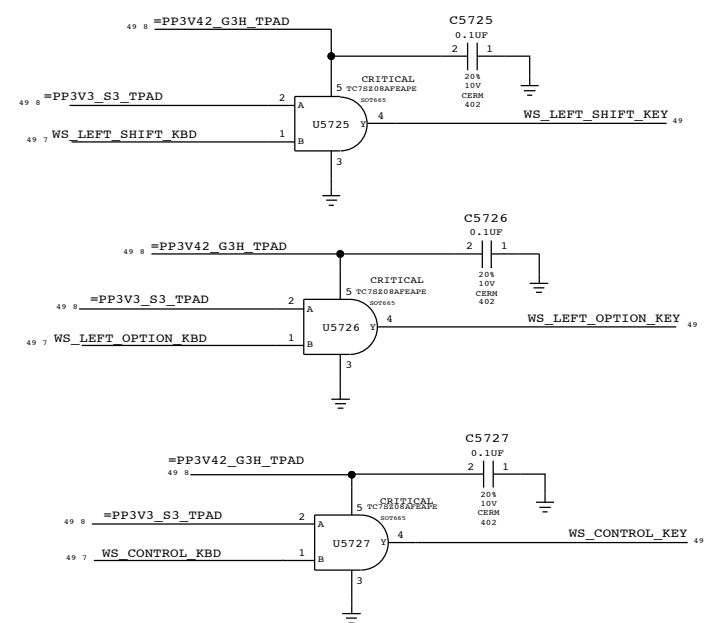
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A	10 OHM	0.204 V	16.32E-6 W
	VOUT	60MA MAX	0.2 OHM	0.6 V	36E-3 W
PSOC	VDD	8MA (TVP)	1.5 OHM	0.012 V	0.72E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

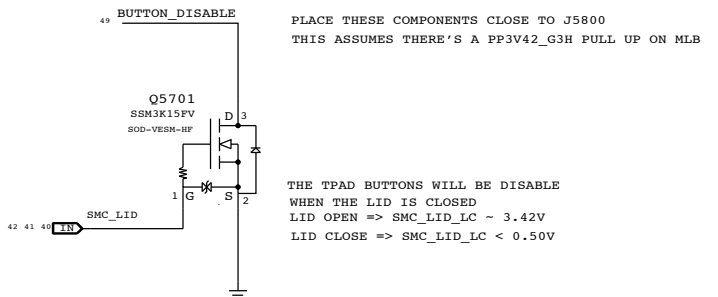
TEST POINTS ARE FOR ON BOARD PROGRAMMING



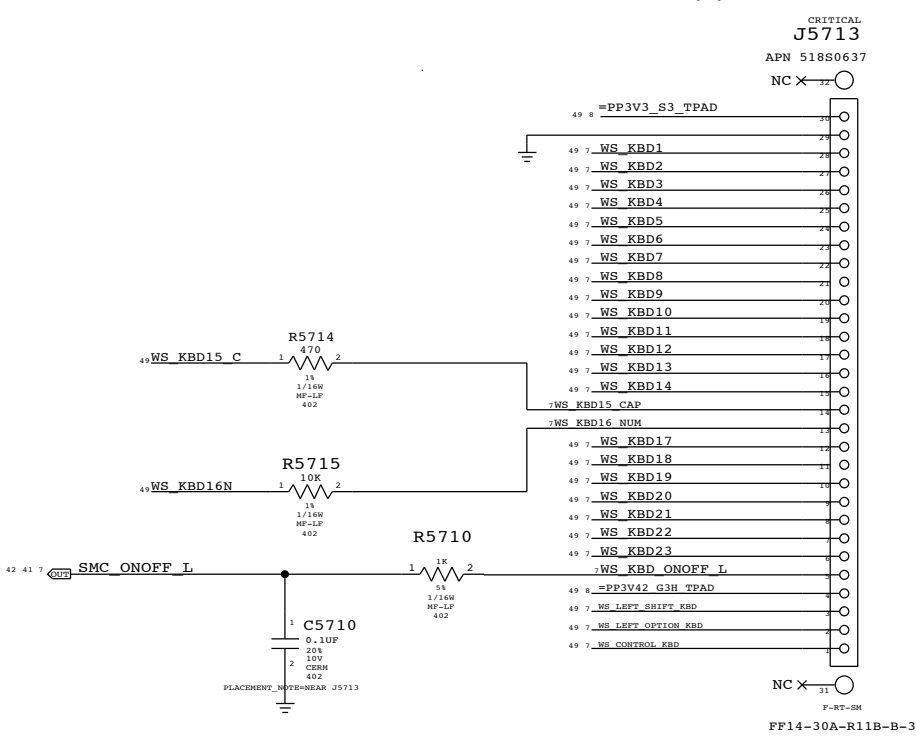
ISOLATION CIRCUIT



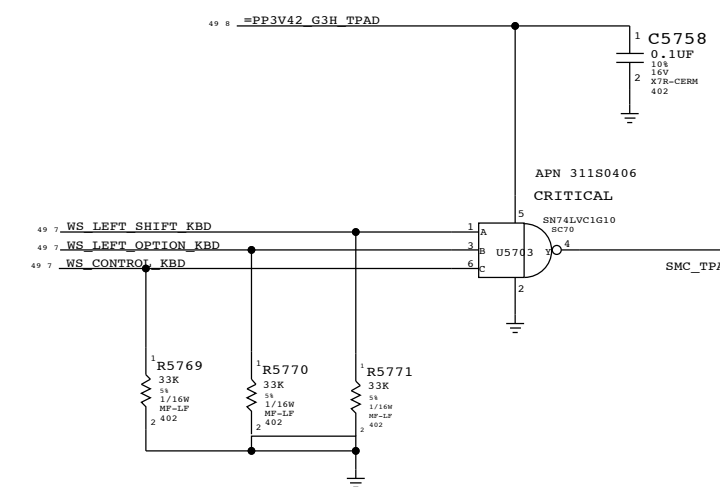
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

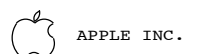


WELLSPRING 1

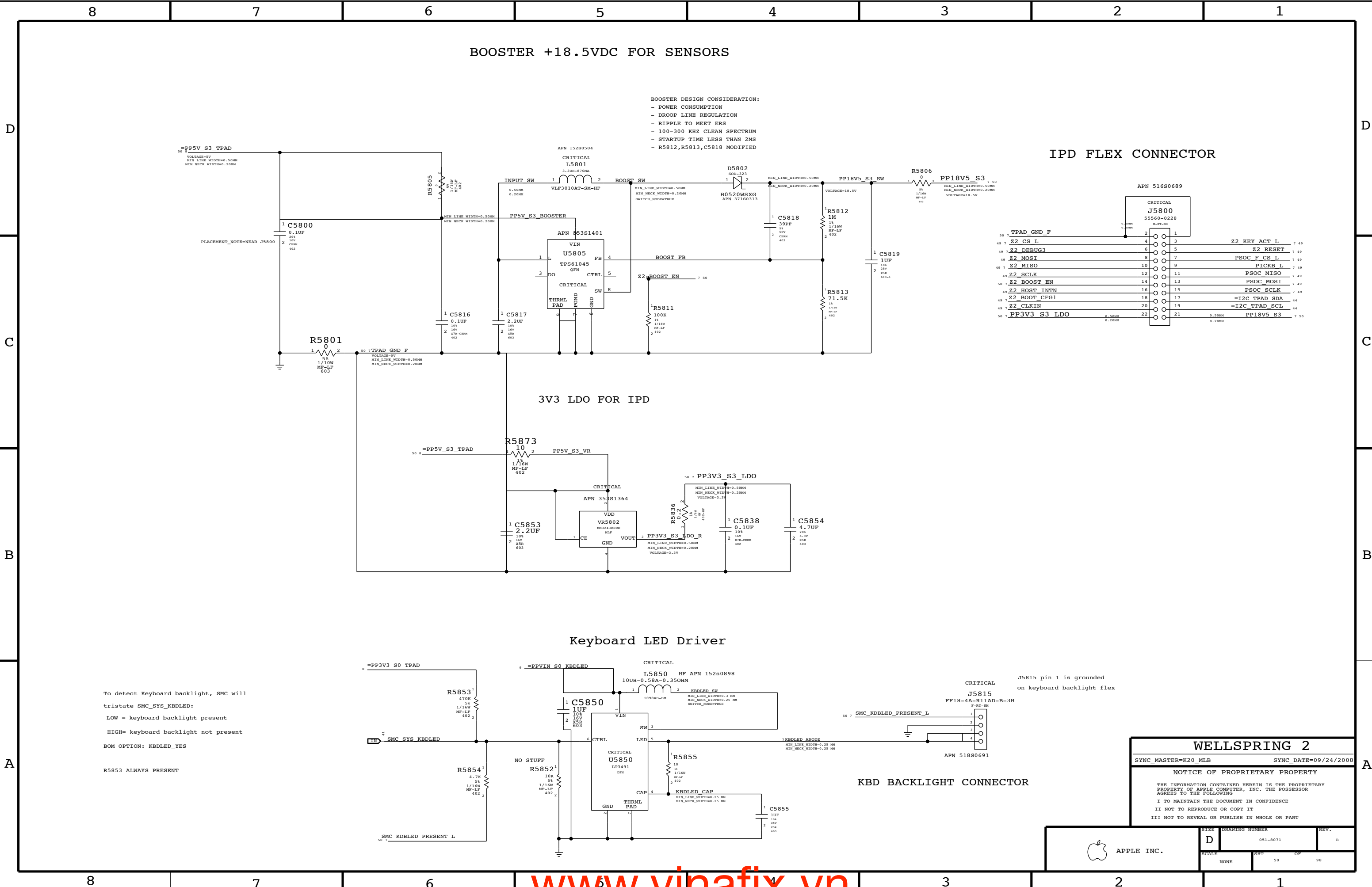
SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

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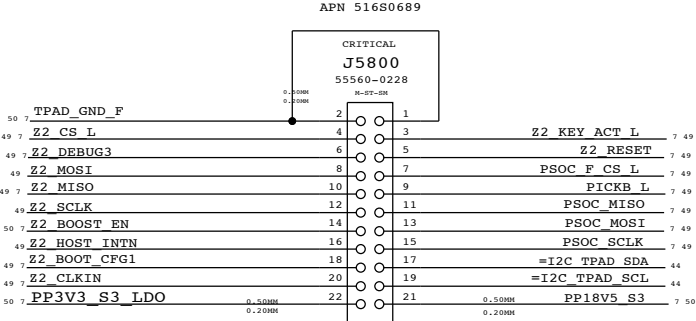
SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	SBT	OF
NONE	49	98



BOOSTER +18.5VDC FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED

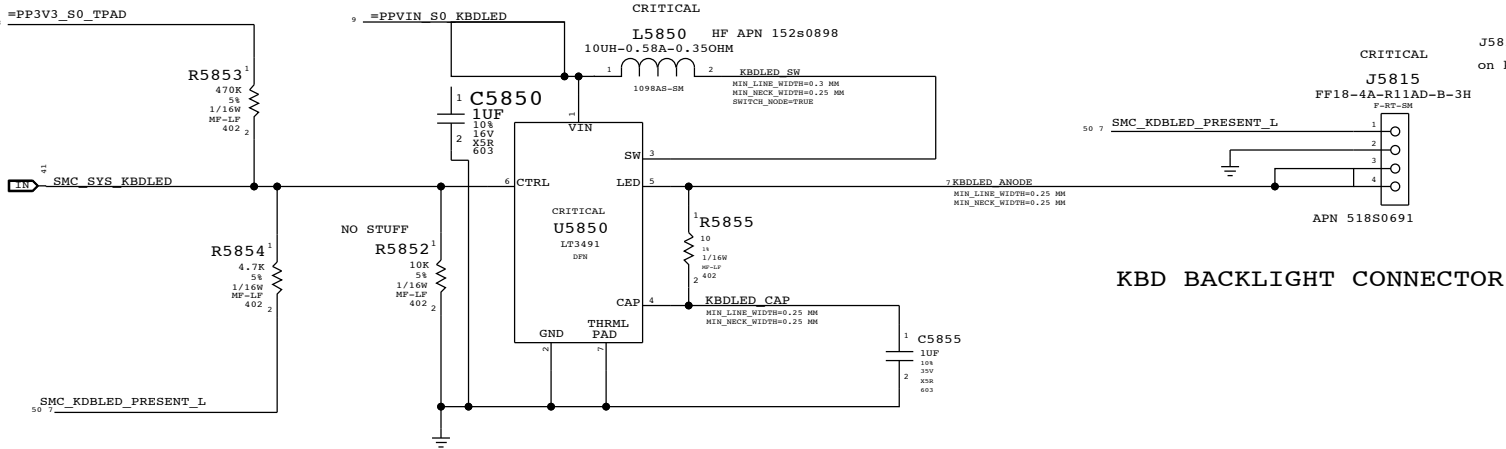
IPD FLEX CONNECTOR



3V3 LDO FOR IPD

Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES
R5853 ALWAYS PRESENT



KBD BACKLIGHT CONNECTOR

WELLSPRING 2

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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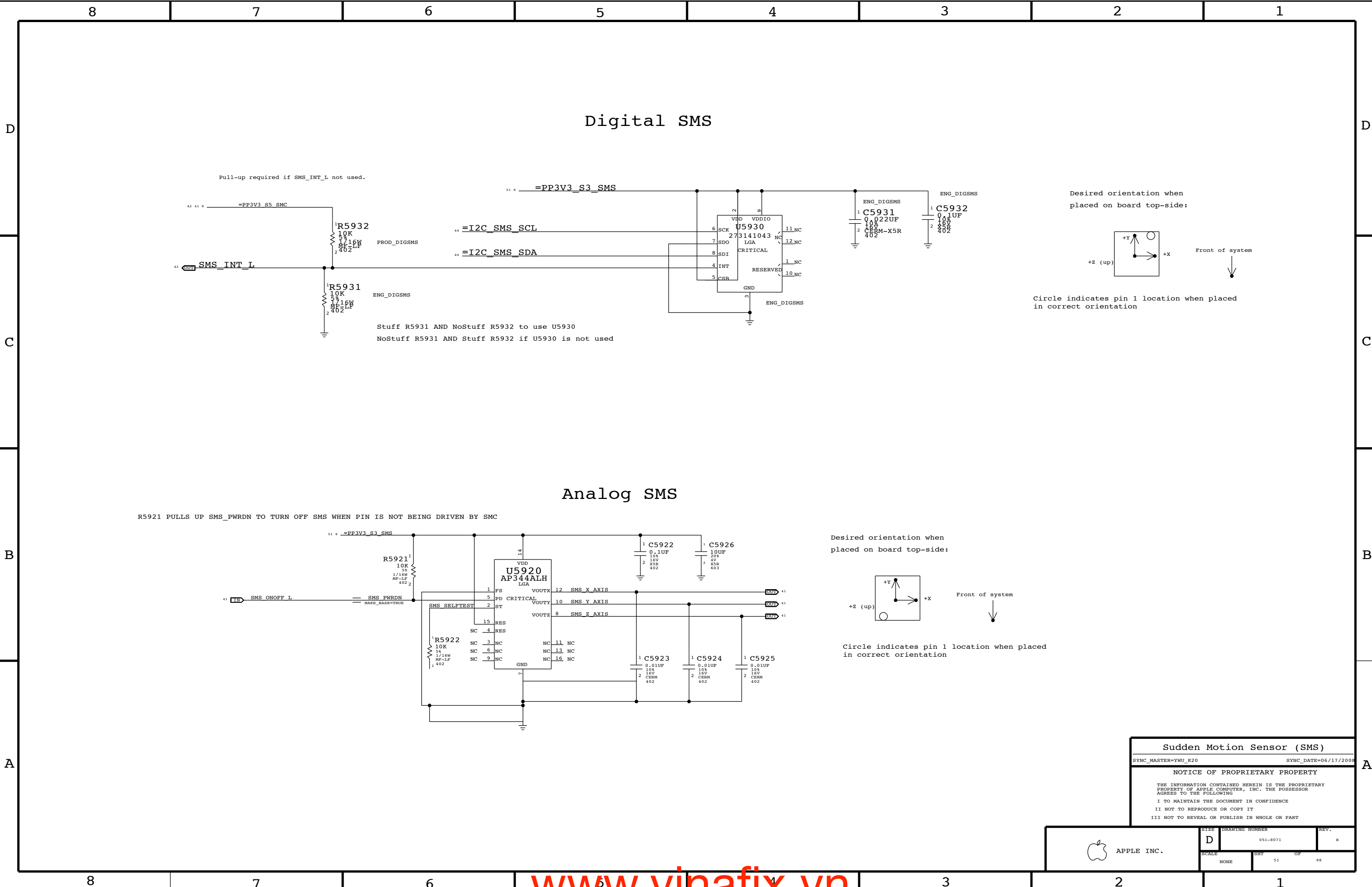
II NOT TO REPRODUCE OR COPY IT

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APPLE INC.

SIZE: D DRAWING NUMBER: 051-8071 REV: B

SCALE: NONE SBT: 50 OF: 98



Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

NOTICE OF PROPRIETARY PROPERTY

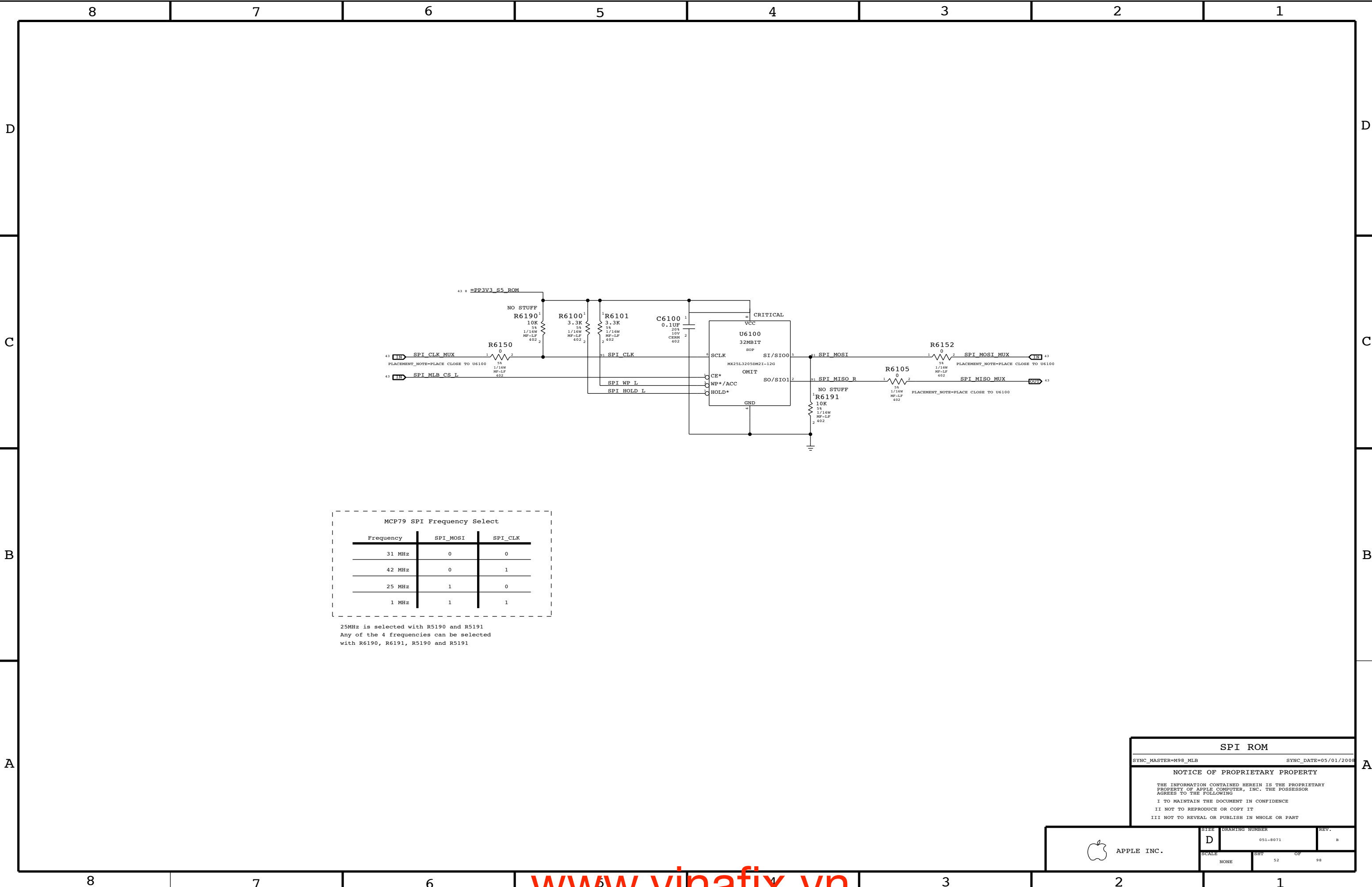
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NONE		51	98



SPI ROM

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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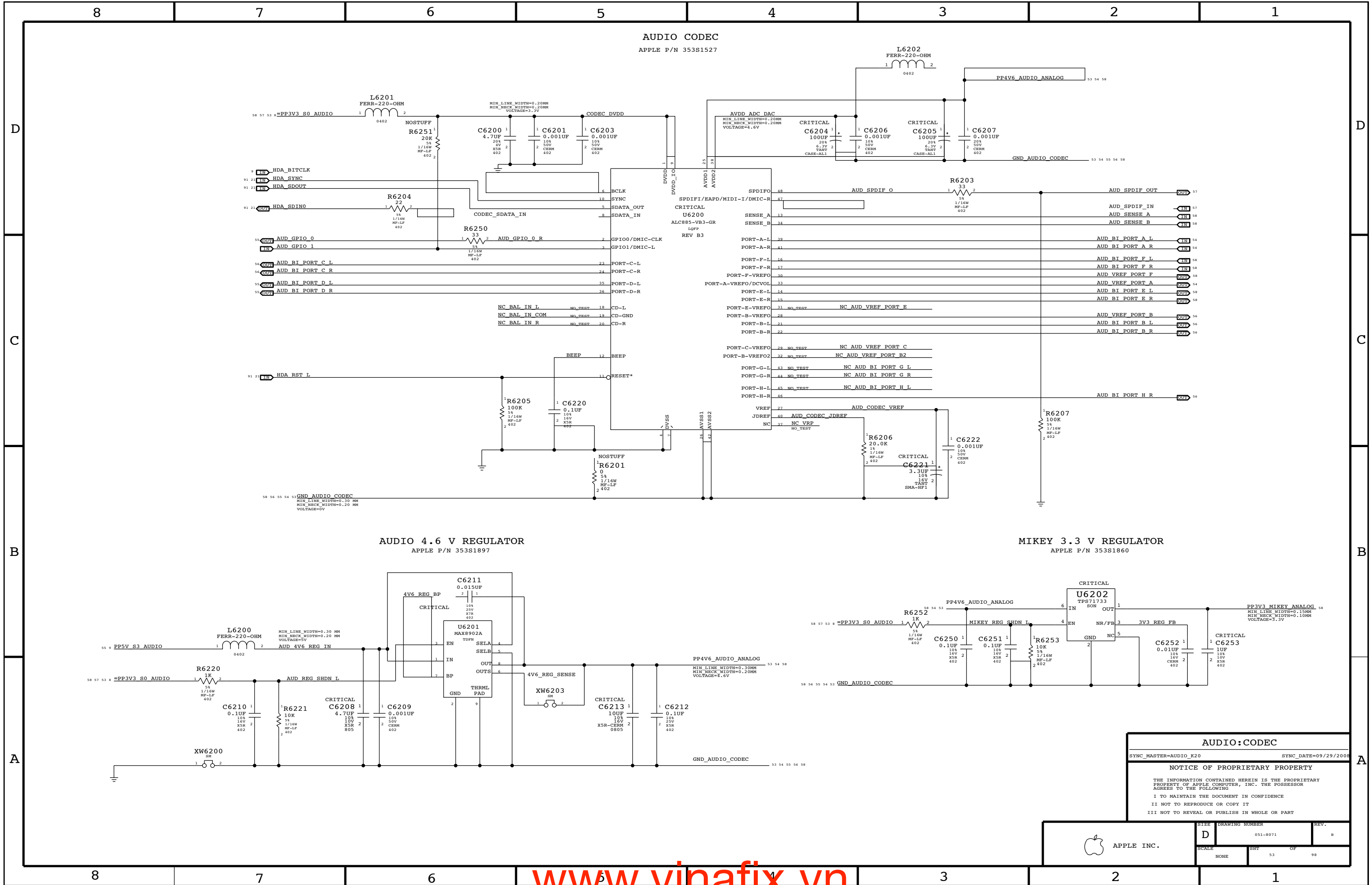
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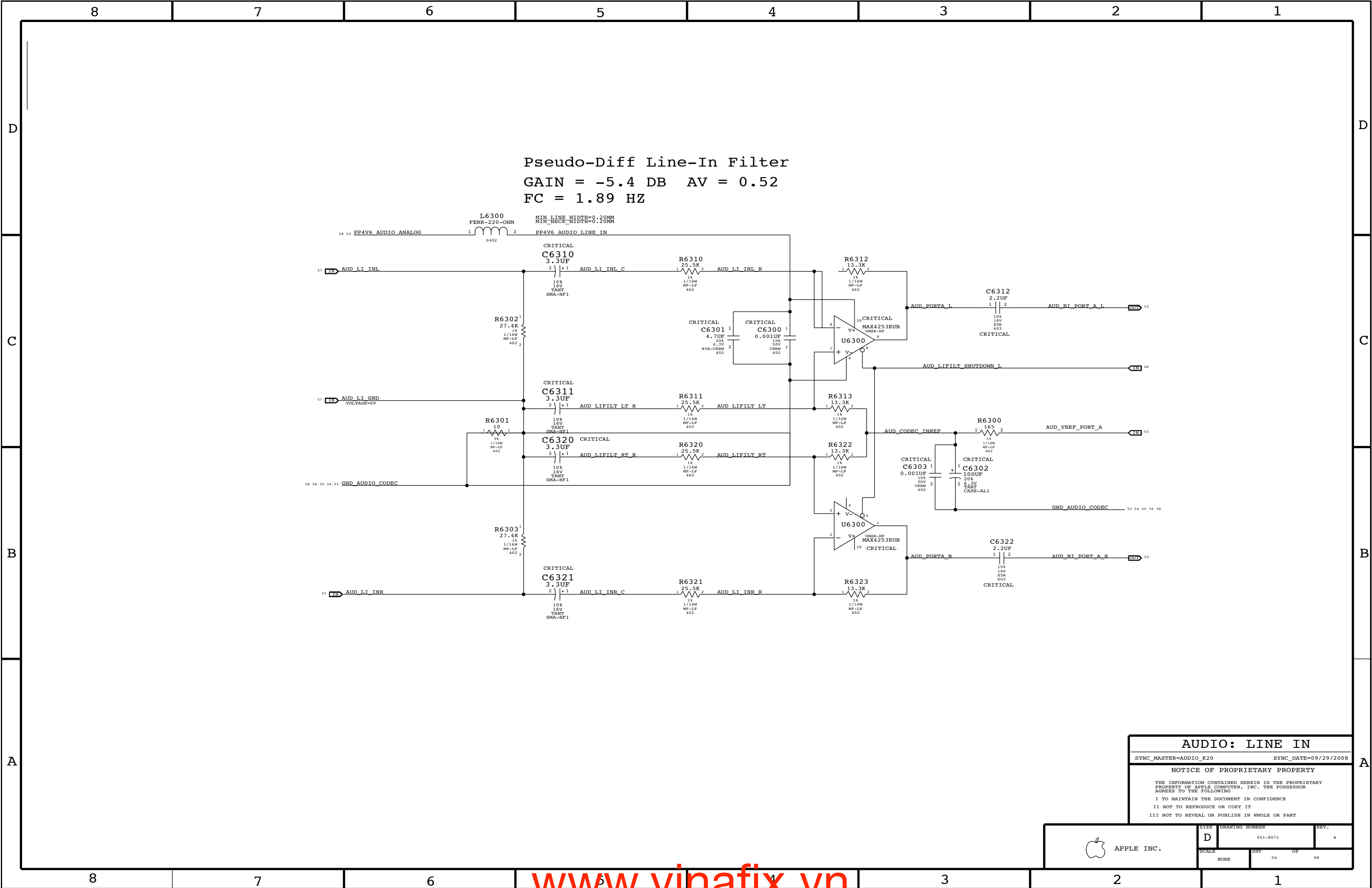
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SIZE	DRAWING NUMBER	REV.
D	051-8071	B
SCALE	52	OF 98





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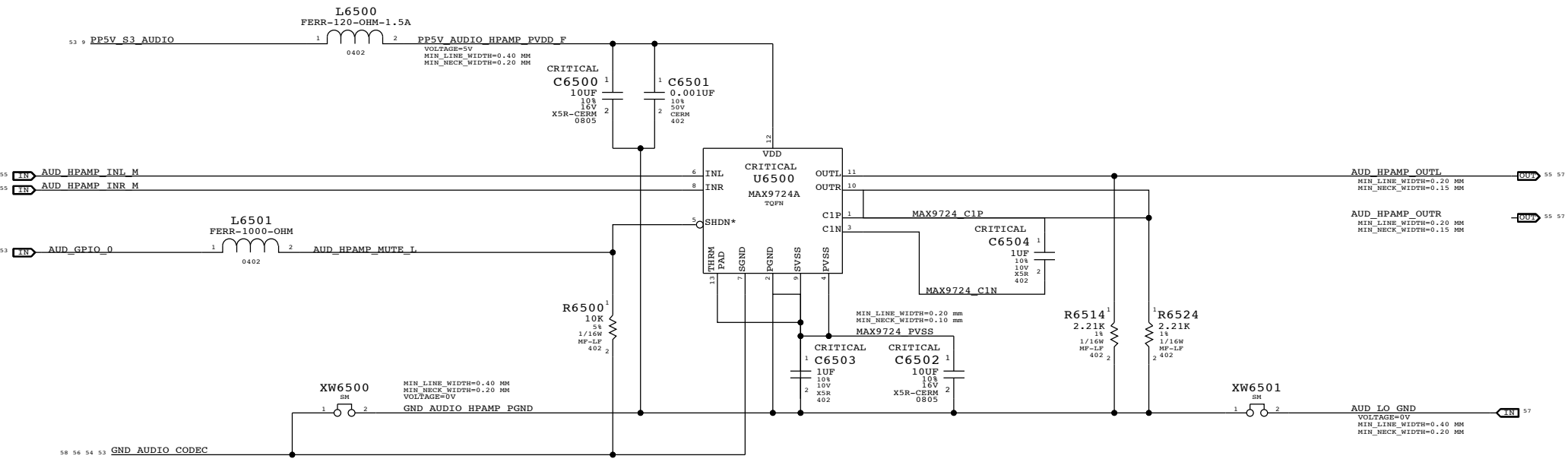
D

C

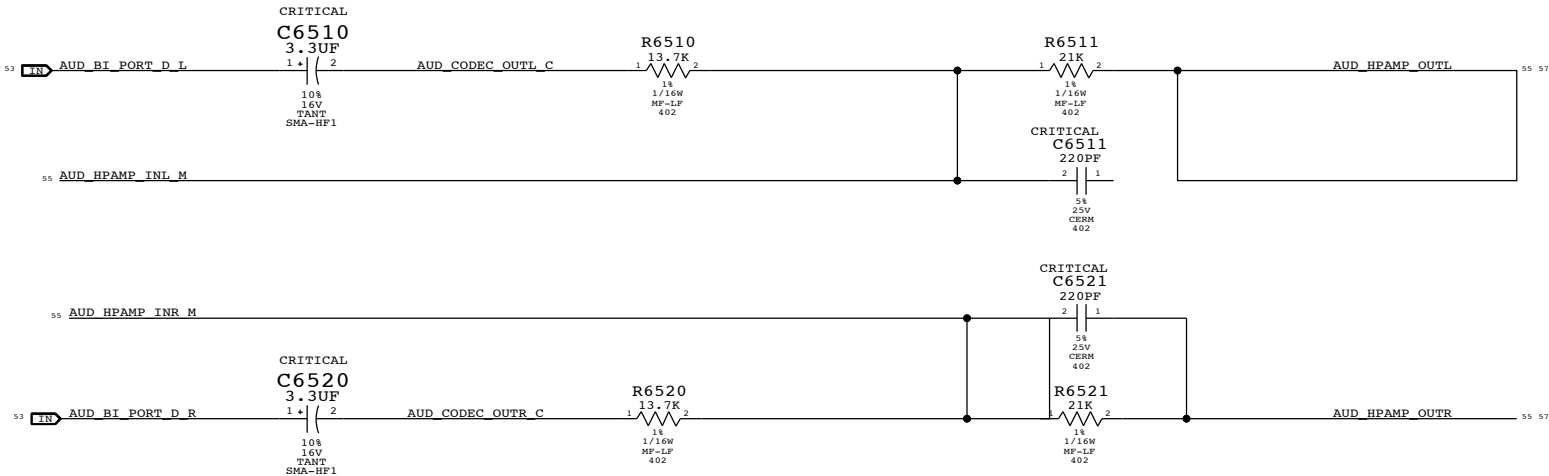
B

A

Headphone Amplifier (MAX9724A)
APN:353S1637



1st Order DAC Filter
HP:3.52 HZ LP:34 KHZ
VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

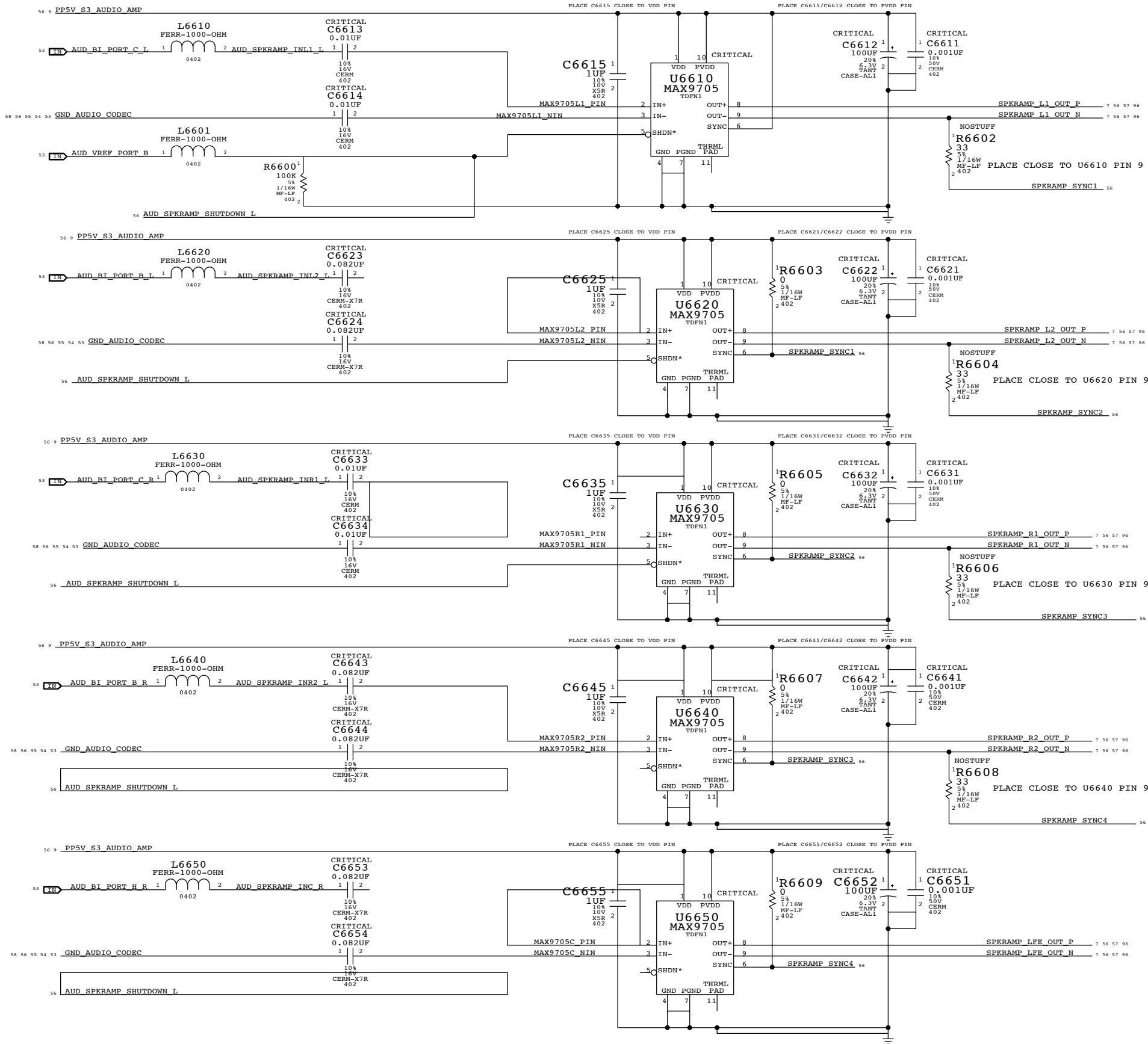
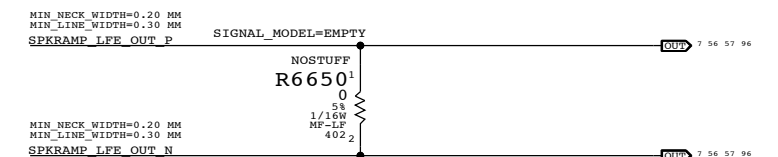
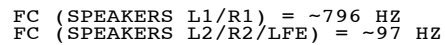
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SCALE		55	98
NONE			



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AUDIO JACK 1 LO/HP JACK, SPDIF TX

MIC CONNECTOR
APN: 518S0520

SPEAKER CONNECTORS
APN: 518S0521

APN: 518S0672

AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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SIZE: DRAWING NUMBER

D

051-8071

REV.

B

SCALE

NONE

57

OF

98

8	7	6	5	4	3	2	1
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C

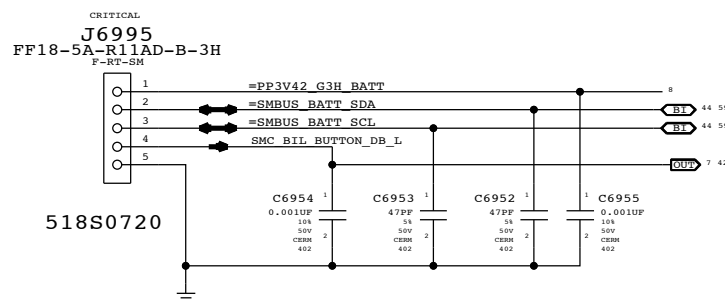
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A



B

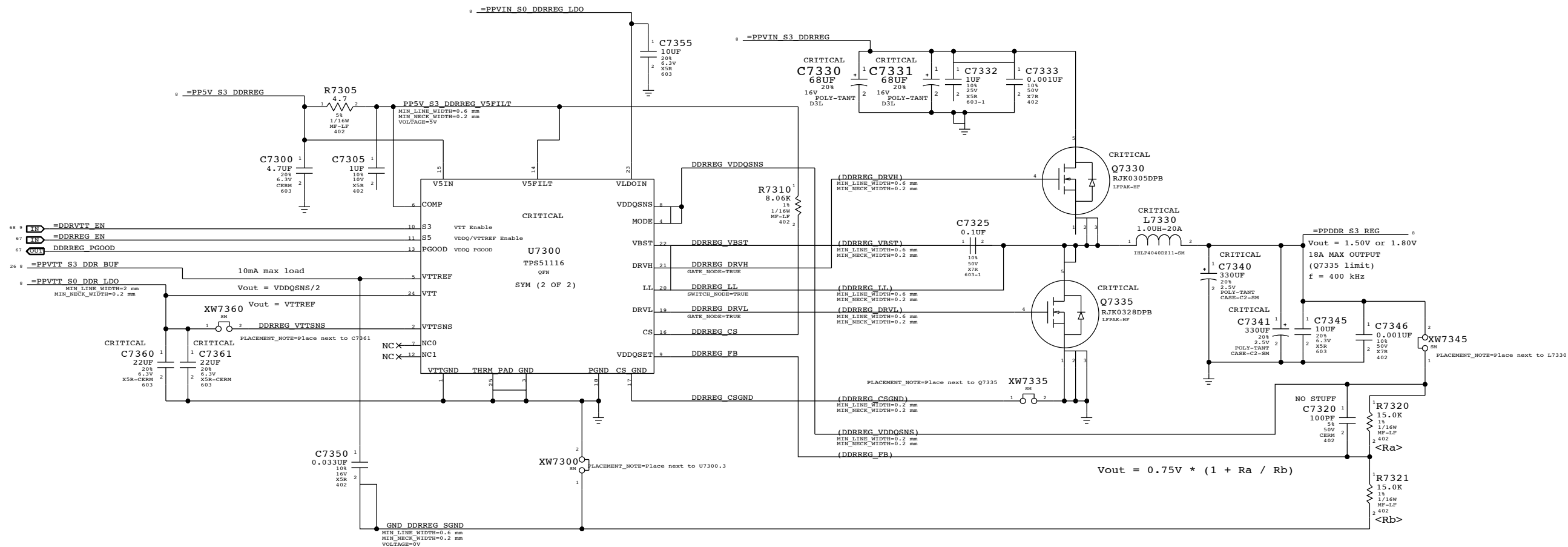
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98







1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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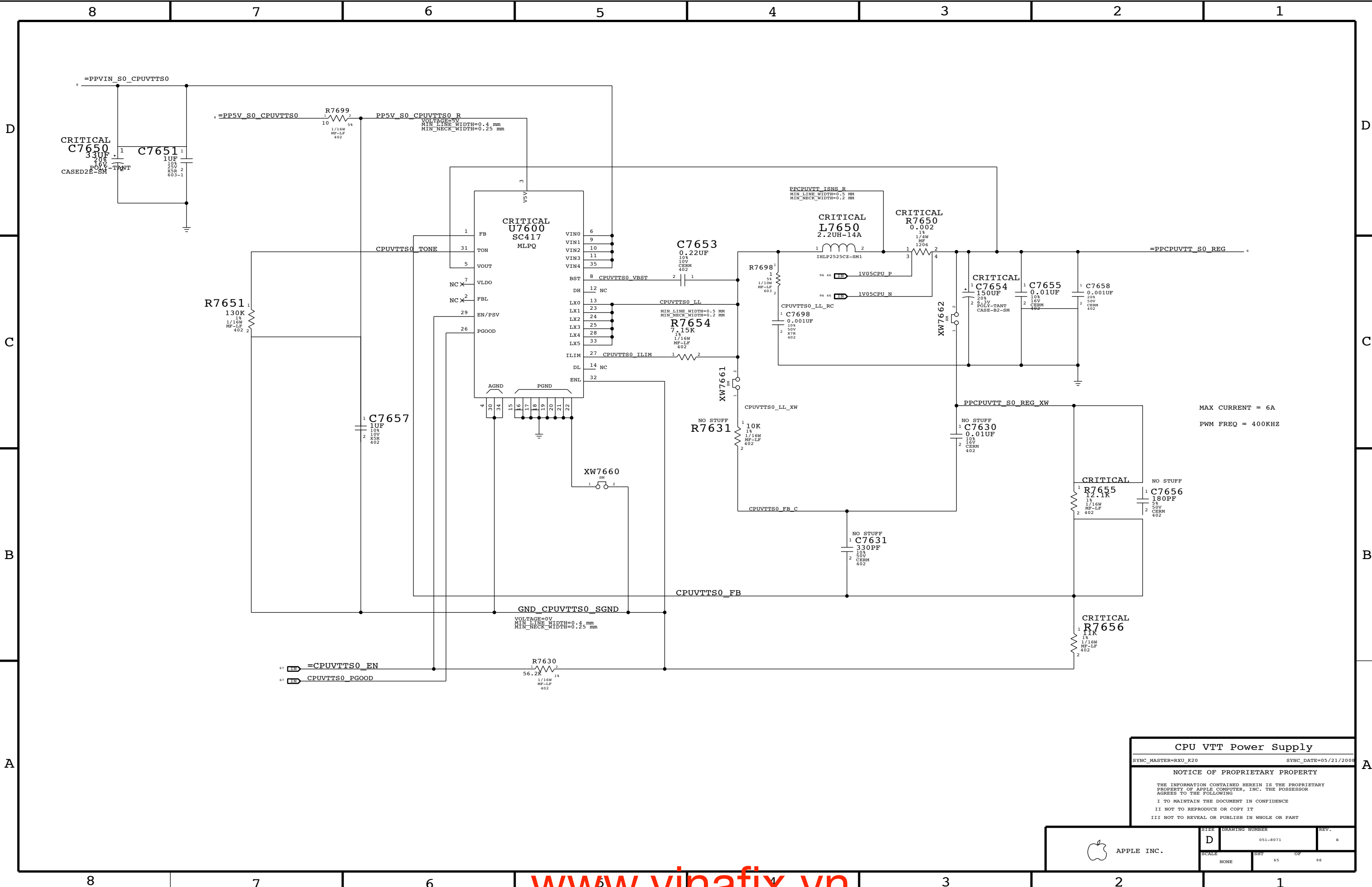
NONE

SBT

63

OF

98



CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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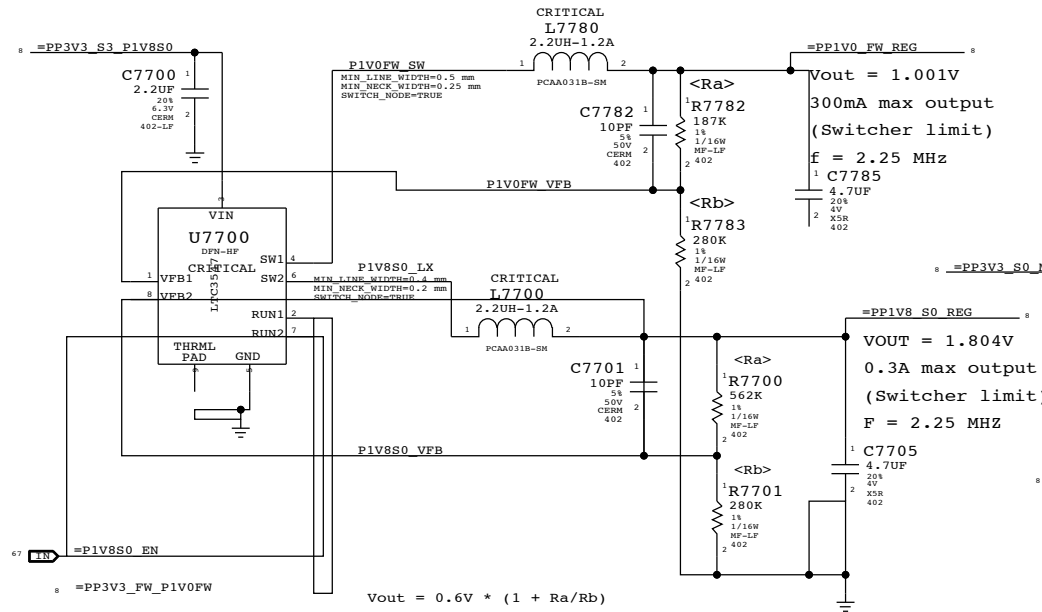
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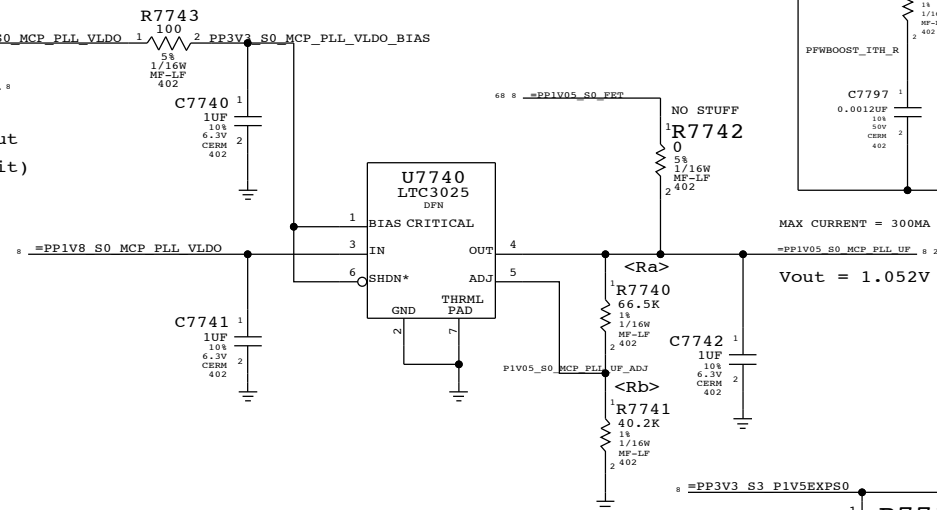
APPLE INC.	DRAWING NUMBER		REV.
	D	051-8071	B
SCALE		SBT	OF
NONE		65	98

1.8V S0 Switcher / 1.0VFW SWITCHER

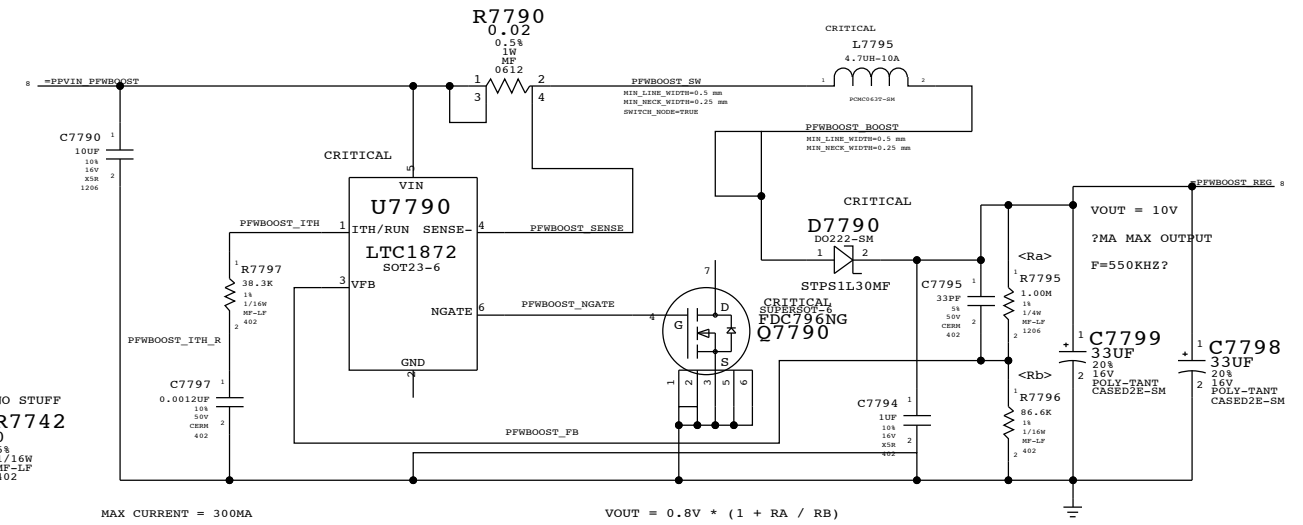
S5 power required for output discharge feature



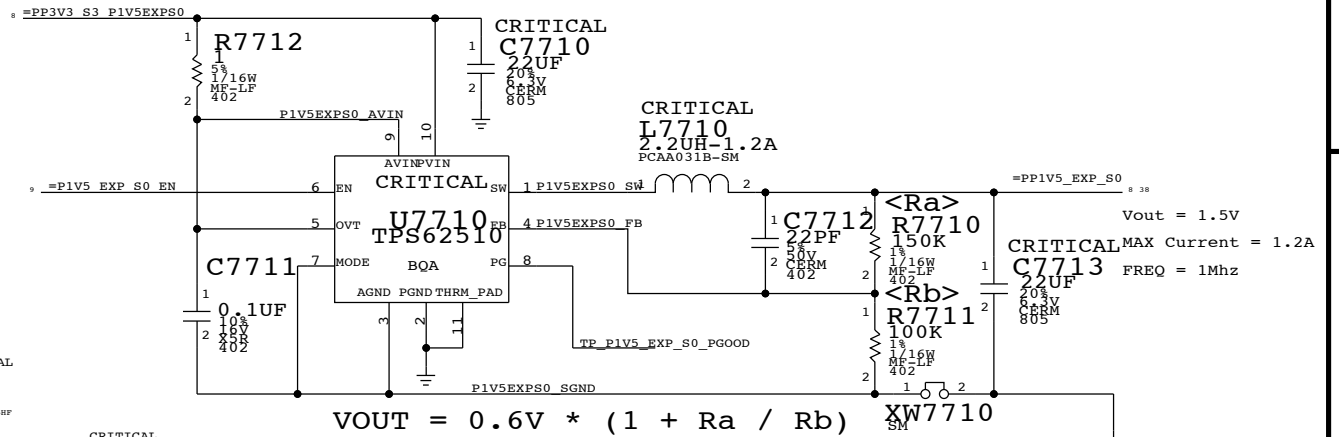
MCP79 PLL VLDO



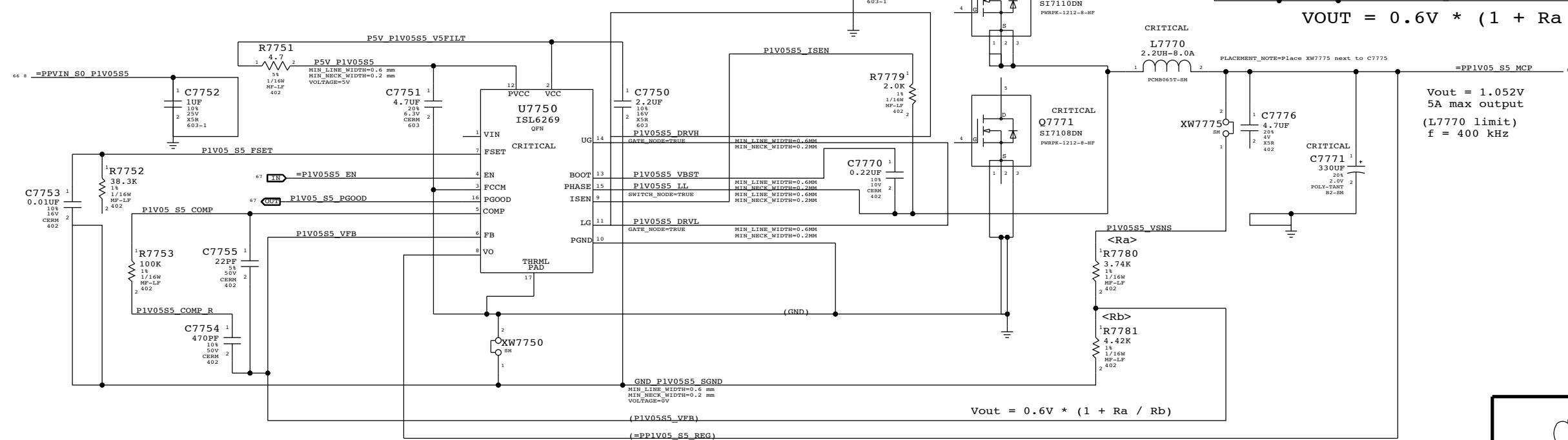
FW BOOST POWER



EXPRESSCARD 1.5V_S0 SUPPLY



MCP 1.05V AUXC Supply



Misc Power Supplies

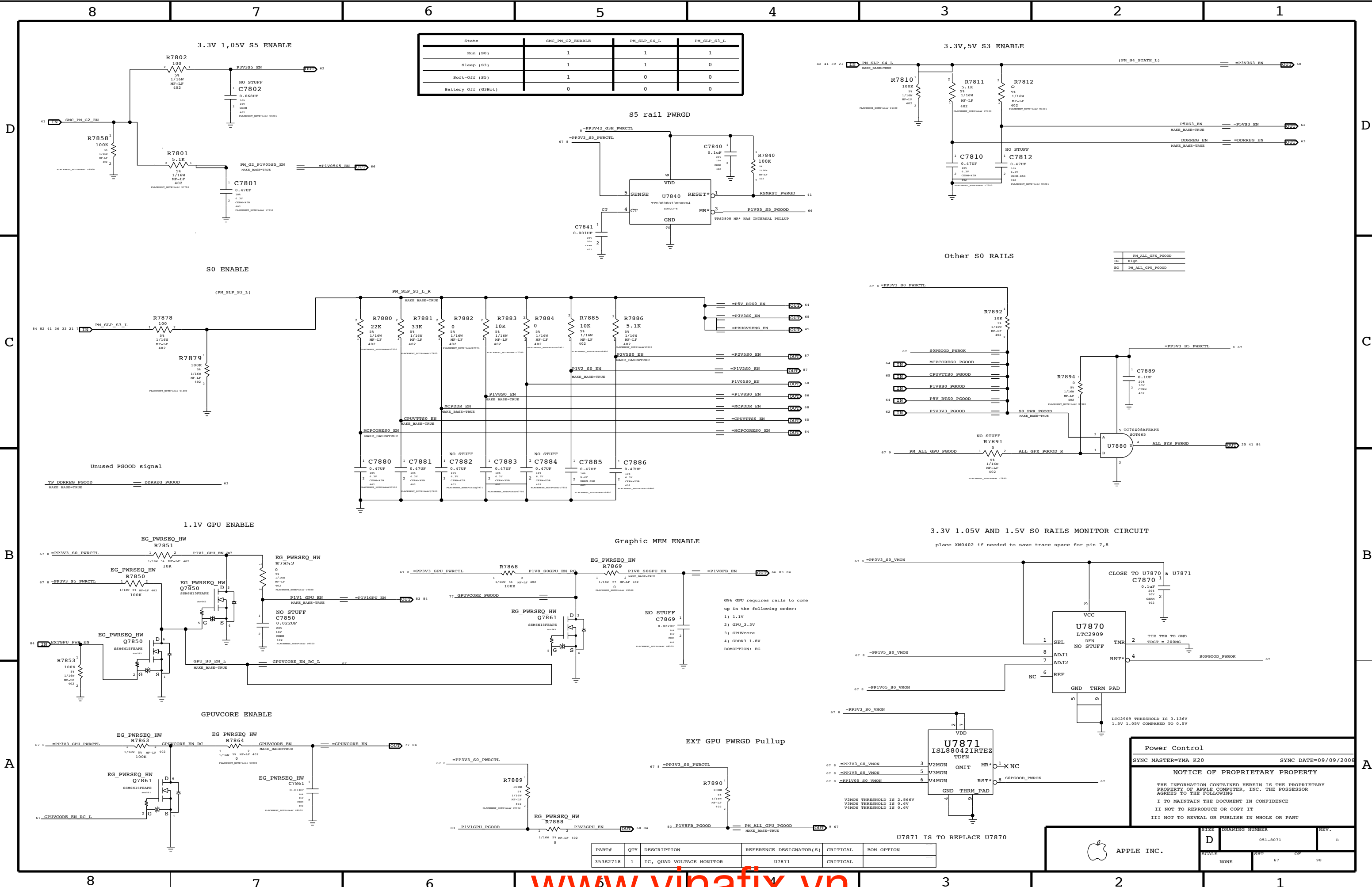
SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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SCALE	DATE	REV.
NONE	051-8071	B



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

S5 rail PWRGD

3.3V,5V S3 ENABLE

S0 ENABLE

Other S0 RAILS

Graphic MEM ENABLE

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

1.1V GPU ENABLE

EXT GPU PWRGD Pullup

Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

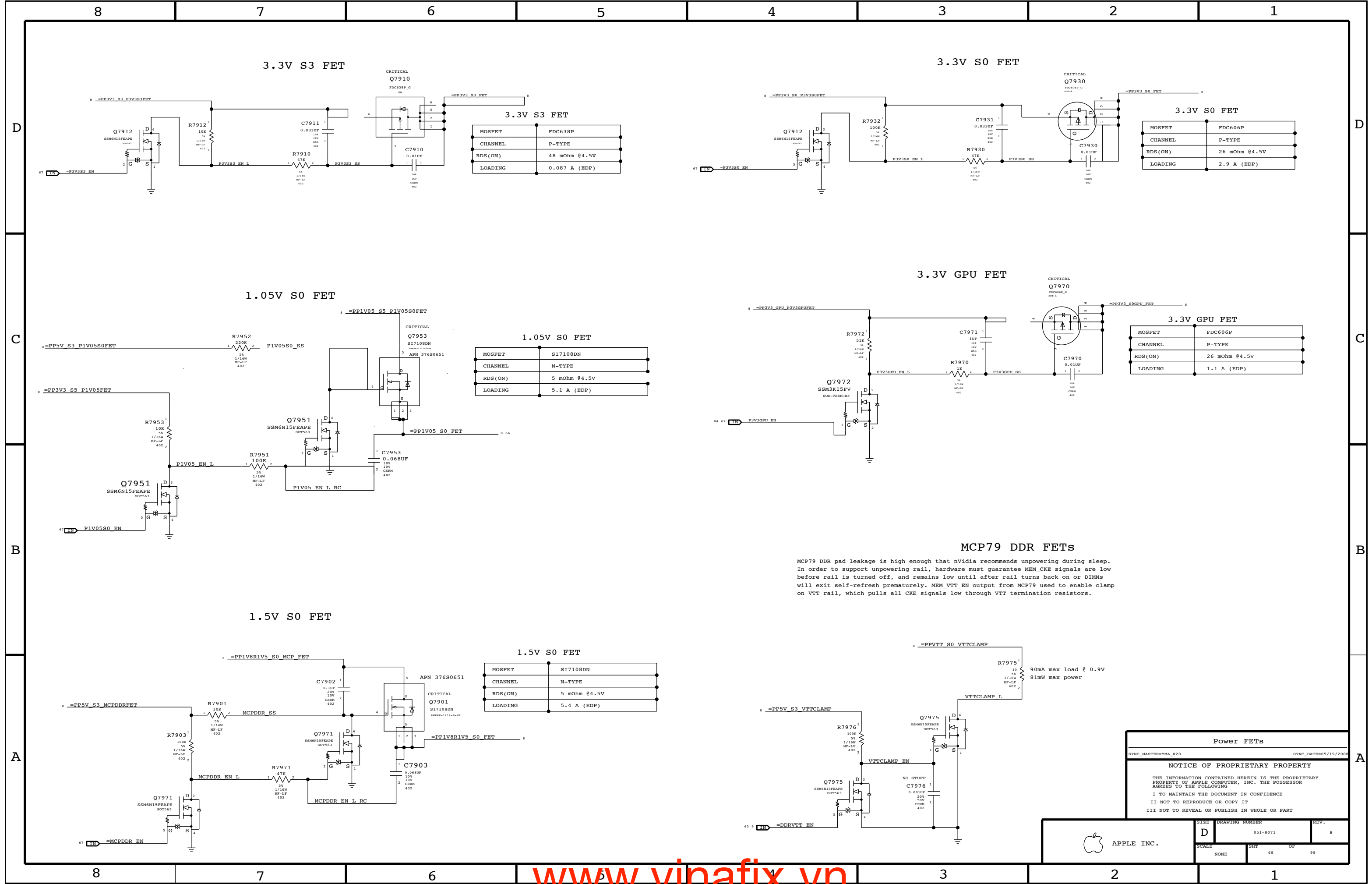
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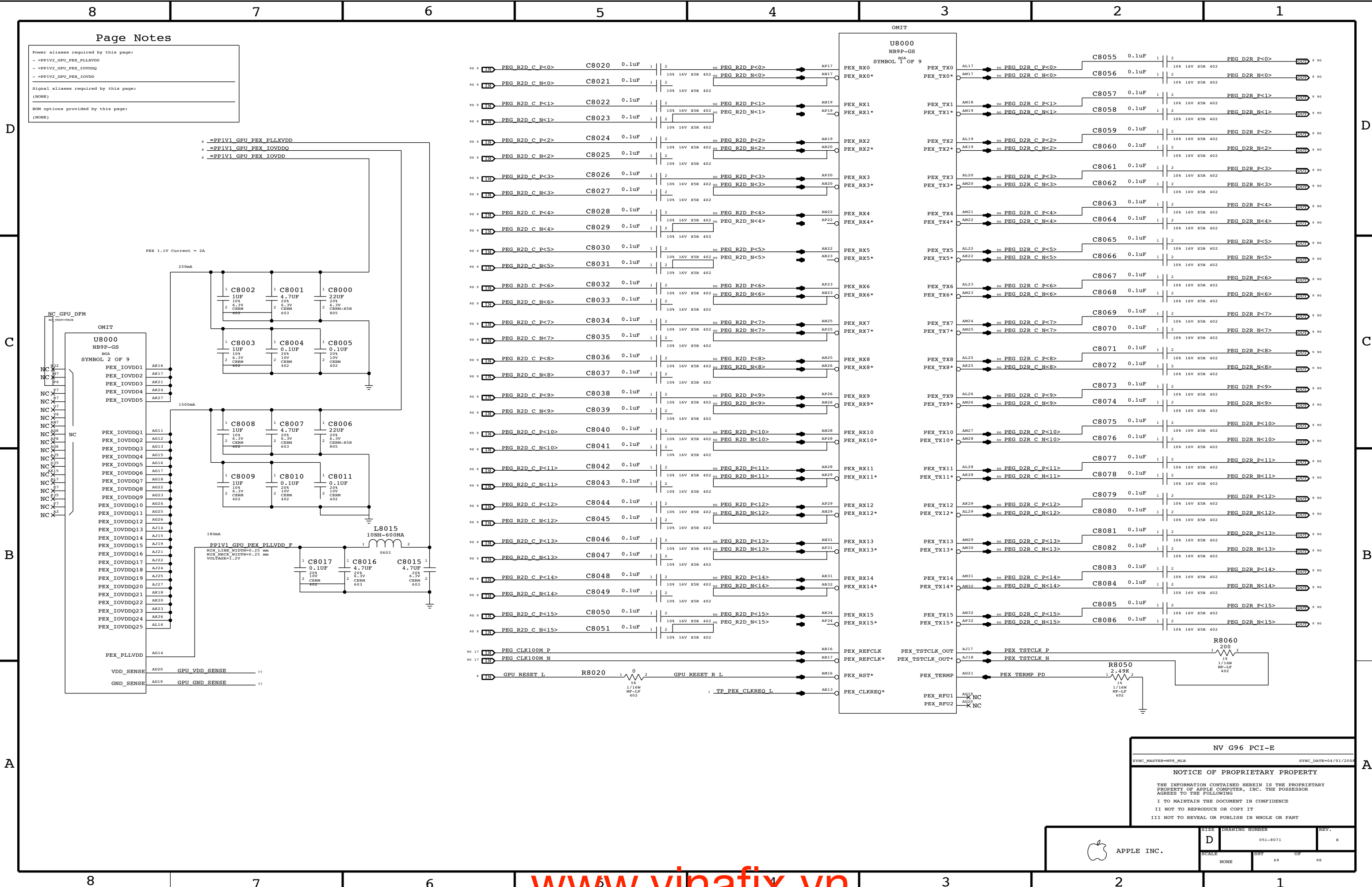
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2718	1	IC, QUAD VOLTAGE MONITOR	U7871	CRITICAL	





Page Notes

Power aliases required by this page:

- =PP1V2_GPU_PEX_PLLVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NV G96 PCI-E

SYNC_MASTER=M98_NL8 SYNC_DATE=04/01/2008

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APPLE INC.

DRAWING NUMBER 051-8071

SCALE NONE SBT 69 OF 98

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU

- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:

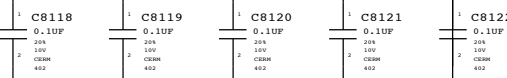
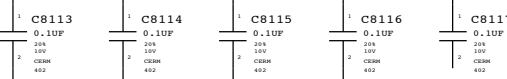
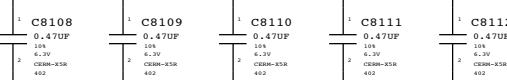
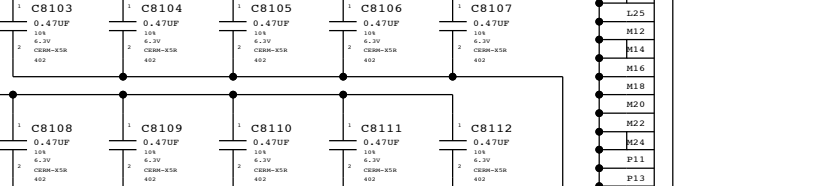
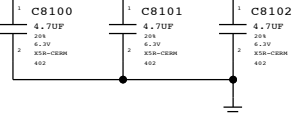
(NONE)

BOM options provided by this page:

(NONE)

=PPVCORE_GPU

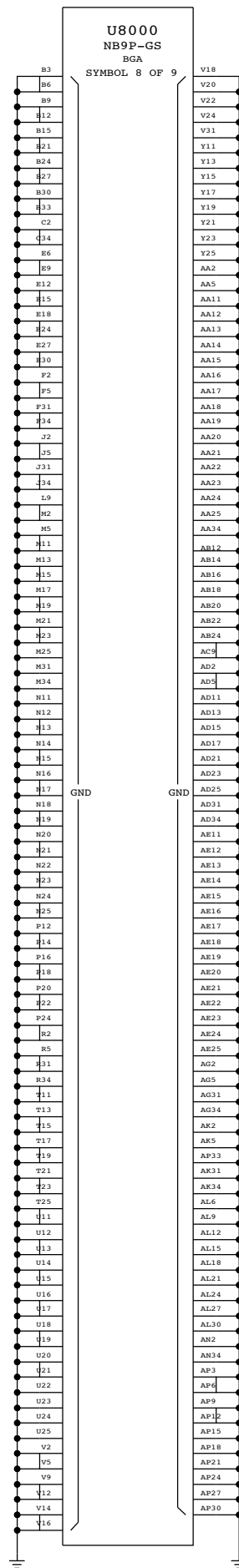
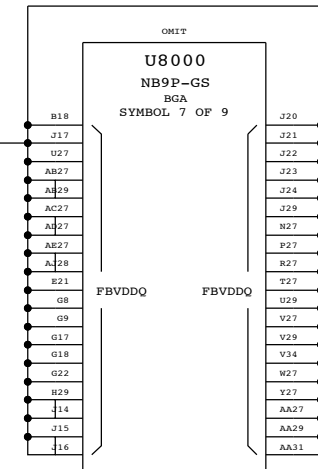
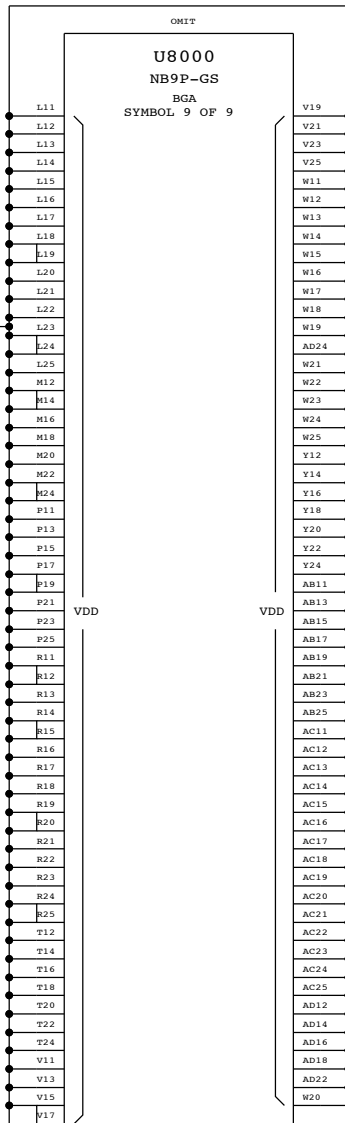
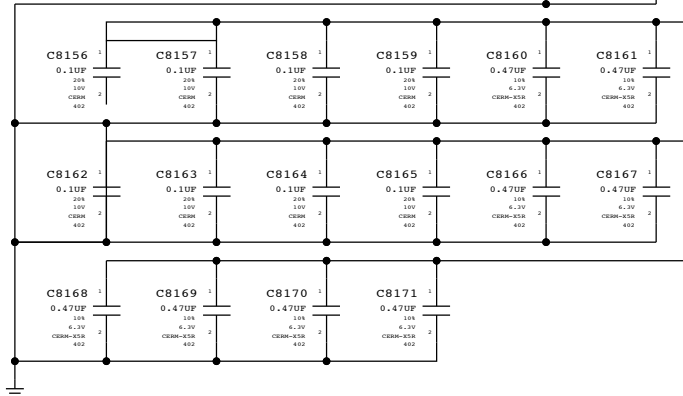
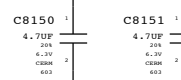
???A @ ???MHz Core/Mem Clk for VDD



=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3



NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLS

SYNC_DATE=04/01/2008

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APPLE INC.

SIZE: DRAWING NUMBER

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B

SCALE

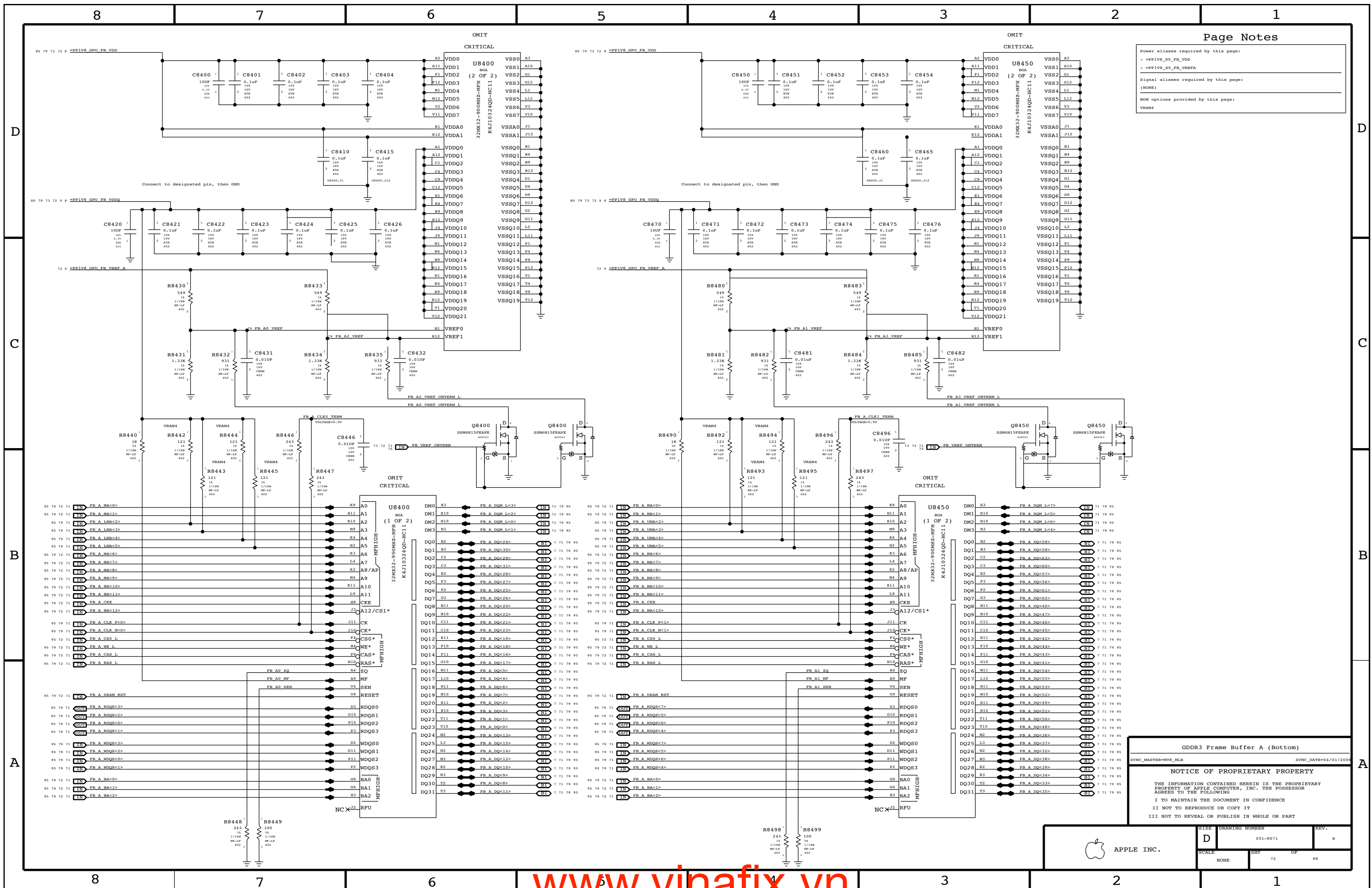
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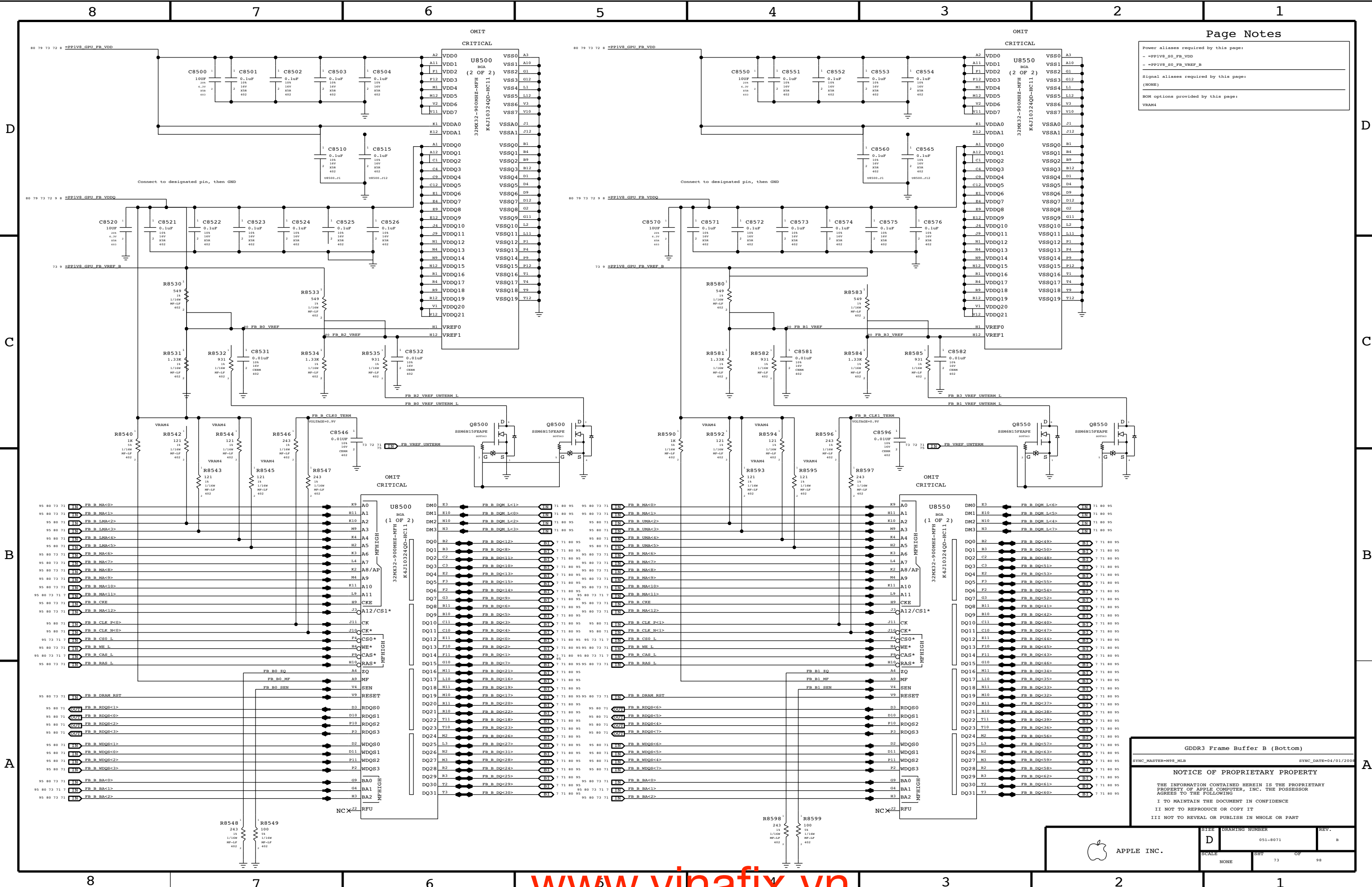
SHEET

70

OF

98





Page Notes

Power aliases required by this page:
- ~PP1V8_S0_FB_VDD
- ~PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer B (Bottom)

SYNC MASTER=M98_MLB SYNC_DATE=04/01/2008

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	051-8071		B
SCALE		80% OF	98

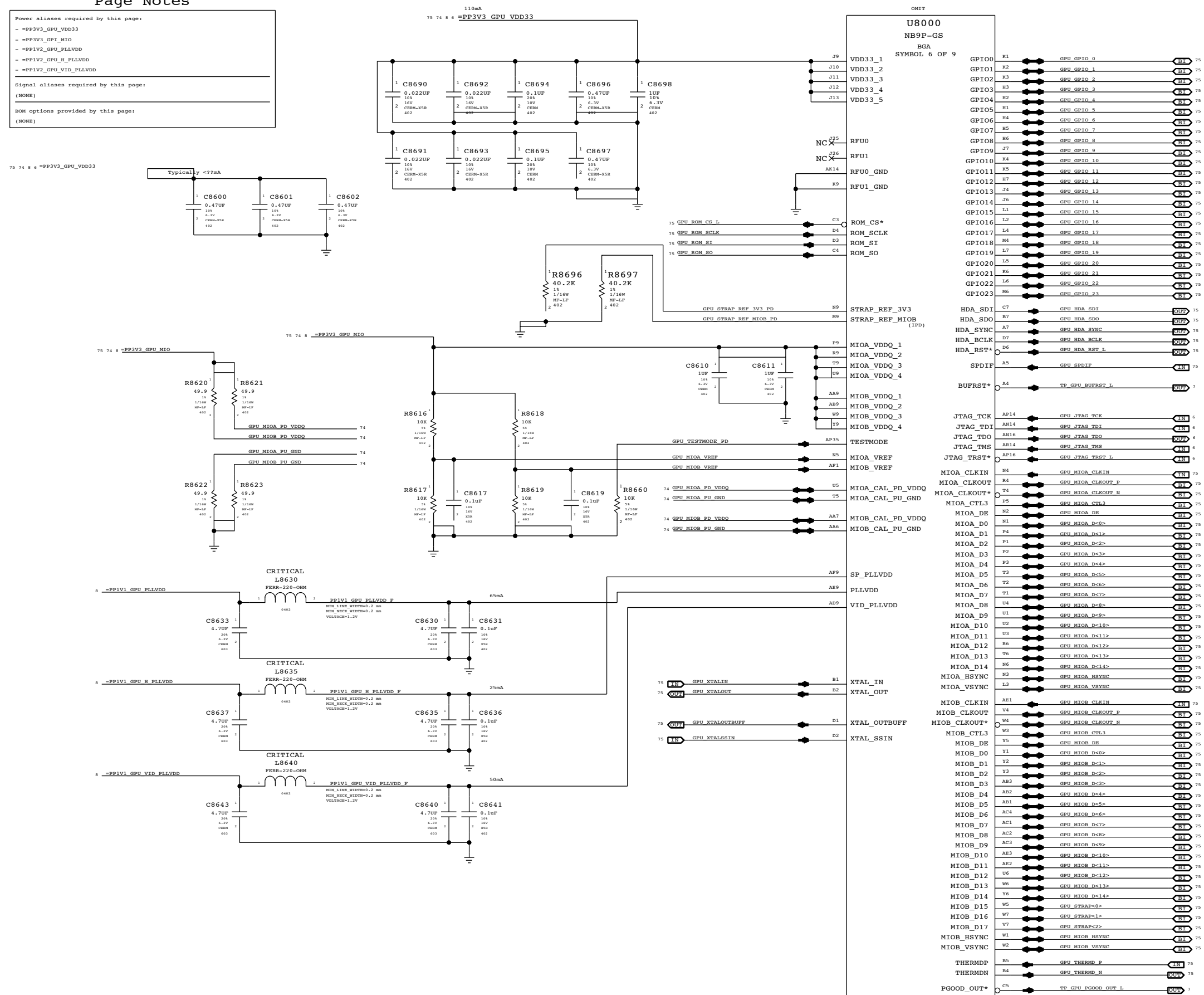
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Power aliases required by this page:
~ =FP3V3_GPU_VDD33
~ =FP3V3_GPU_MIO
~ =FP1V2_GPU_FLLVDD
~ =FP1V2_GPU_R_FLLVDD
~ =FP1V2_GPU_VID_FLLVDD
```

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



OF 9	GPIO0	K1		GPU_GPIO_0		75
	GPIO1	K2		GPU_GPIO_1		75
	GPIO2	K3		GPU_GPIO_2		75
	GPIO3	K3		GPU_GPIO_3		75
	GPIO4	H2		GPU_GPIO_4		75
	GPIO5	H1		GPU_GPIO_5		75
	GPIO6	H4		GPU_GPIO_6		75
	GPIO7	H5		GPU_GPIO_7		75
	GPIO8	H6		GPU_GPIO_8		75
	GPIO9	J7		GPU_GPIO_9		75
	GPIO10	K4		GPU_GPIO_10		75
	GPIO11	K5		GPU_GPIO_11		75
	GPIO12	J8		GPU_GPIO_12		75
	GPIO13	H4		GPU_GPIO_13		75
	GPIO14	L1		GPU_GPIO_14		75
	GPIO15	L1		GPU_GPIO_15		75
	GPIO16	L2		GPU_GPIO_16		75
	GPIO17	L4		GPU_GPIO_17		75
	GPIO18	M4		GPU_GPIO_18		75
	GPIO19	L7		GPU_GPIO_19		75
	GPIO20	L5		GPU_GPIO_20		75
	GPIO21	K6		GPU_GPIO_21		75
	GPIO22	M6		GPU_GPIO_22		75
	GPIO23	L6		GPU_GPIO_23		75
	HDA_SDI	C7		GPU_HDA_SDI		75
	HDA_SDO	A7		GPU_HDA_SDO		75
	HDA_SYNC	D7		GPU_HDA_SYNC		75
	HDA_BCLK	D7		GPU_HDA_BCLK		75
	HDA_RST*	D6		GPU_HDA_RST_L		75
	SPDIF			GPU_SPDIF		75
	BUFRST*	A4		TP_GPU_BUFRST_L		7
	JTAG_TCK	AP14		GPU_JTAG_TCK		6
	JTAG_TDI	AN14		GPU_JTAG_TDI		6
	JTAG_TDO	AN16		GPU_JTAG_TDO		6
	JTAG_TMS	AN14		GPU_JTAG_TMS		6
	JTAG_TRST*	AP16		GPU_JTAG_TRST_L		6
	MIOA_CLKIN	N4		GPU_MIOA_CLKIN		75
	MIOA_CLKOUT	R4		GPU_MIOA_CLKOUT_P		75
	MIOA_CLKOUT*	T4		GPU_MIOA_CLKOUT_N		75
	MIOA_CTL3	P5		GPU_MIOA_CTL3		75
	MIOA_DE	N2		GPU_MIOA_DE		75
	MIOA_D0	N1		GPU_MIOA_D<0>		75
	MIOA_D1	P1		GPU_MIOA_D<1>		75
	MIOA_D2	F1		GPU_MIOA_D<2>		75
	MIOA_D3	P2		GPU_MIOA_D<3>		75
	MIOA_D4	F3		GPU_MIOA_D<4>		75
	MIOA_D5	T3		GPU_MIOA_D<5>		75
	MIOA_D6	T2		GPU_MIOA_D<6>		75
	MIOA_D7	U1		GPU_MIOA_D<7>		75
	MIOA_D8	T4		GPU_MIOA_D<8>		75
	MIOA_D9	U1		GPU_MIOA_D<9>		75
	MIOA_D10	U2		GPU_MIOA_D<10>		75
	MIOA_D11	U3		GPU_MIOA_D<11>		75
	MIOA_D12	R6		GPU_MIOA_D<12>		75
	MIOA_D13	T6		GPU_MIOA_D<13>		75
	MIOA_D14	N6		GPU_MIOA_D<14>		75
	MIOA_HSYNC	N3		GPU_MIOA_HSYNC		75
	MIOA_VSYNC	L3		GPU_MIOA_VSYNC		75
	MIOB_CLKIN	VE1		GPU_MIOB_CLKIN		75
	MIOB_CLKOUT	W4		GPU_MIOB_CLKOUT_P		75
	MIOB_CLKOUT*	W4		GPU_MIOB_CLKOUT_N		75
	MIOB_CTL3	W3		GPU_MIOB_CTL3		75
	MIOB_DE	Y5		GPU_MIOB_DE		75
	MIOB_D0	Y1		GPU_MIOB_D<0>		75
	MIOB_D1	Y2		GPU_MIOB_D<1>		75
	MIOB_D2	Y3		GPU_MIOB_D<2>		75
	MIOB_D3	AB3		GPU_MIOB_D<3>		75
	MIOB_D4	AB1		GPU_MIOB_D<4>		75
	MIOB_D5	AR2		GPU_MIOB_D<5>		75
	MIOB_D6	AC4		GPU_MIOB_D<6>		75
	MIOB_D7	AC1		GPU_MIOB_D<7>		75
	MIOB_D8	AC2		GPU_MIOB_D<8>		75
	MIOB_D9	AC3		GPU_MIOB_D<9>		75
	MIOB_D10	AE3		GPU_MIOB_D<10>		75
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	MIOB_D14	W6		GPU_MIOB_D<14>		75
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	MIOB_HSYNC	W1		GPU_MIOB_HSYNC		75
	MIOB_VSYNC	W2		GPU_MIOB_VSYNC		75
	THERMDP	B4		GPU_THERM_P		75
	THERMDN	B5		GPU_THERM_N		75
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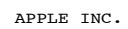
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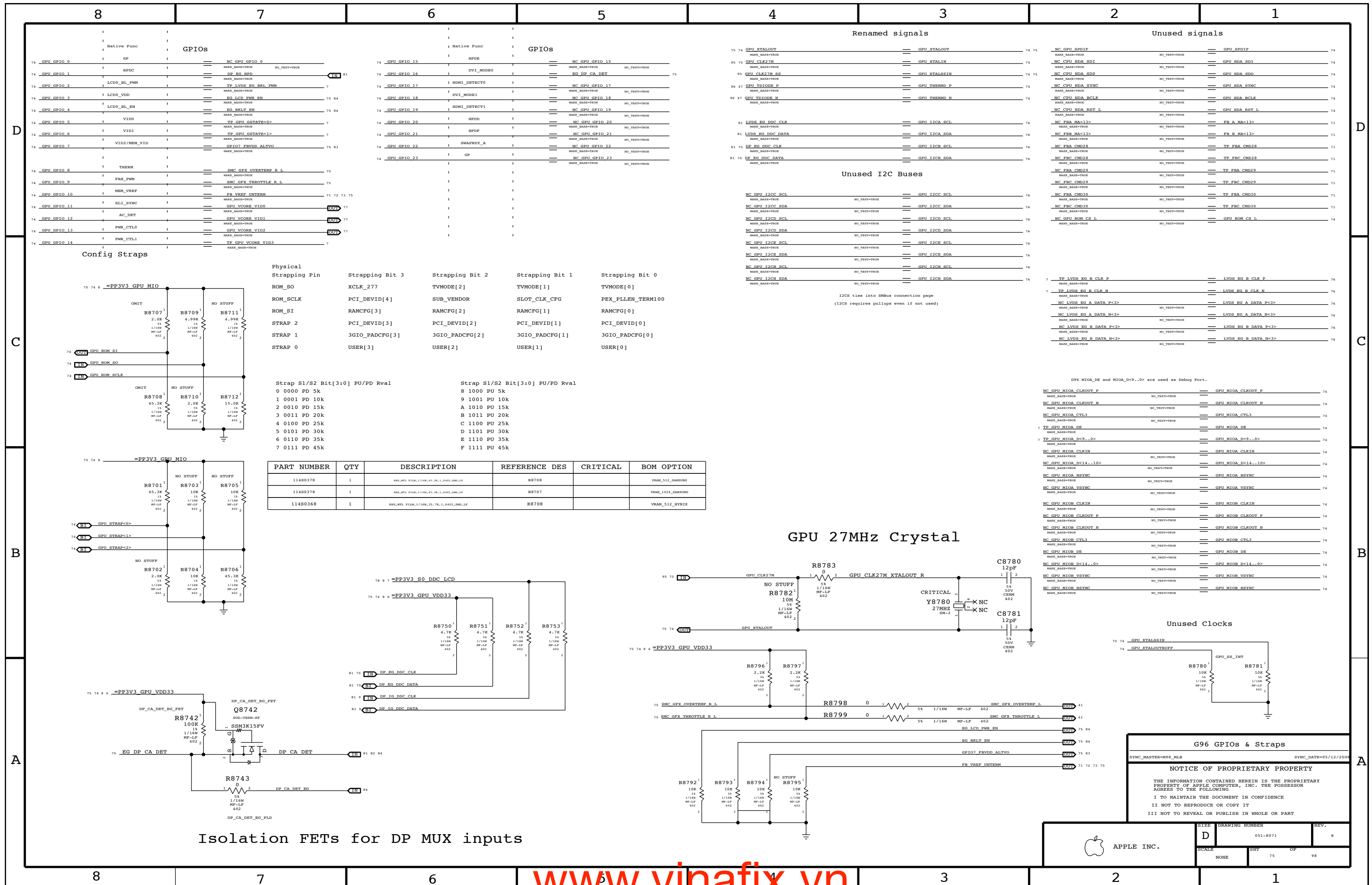
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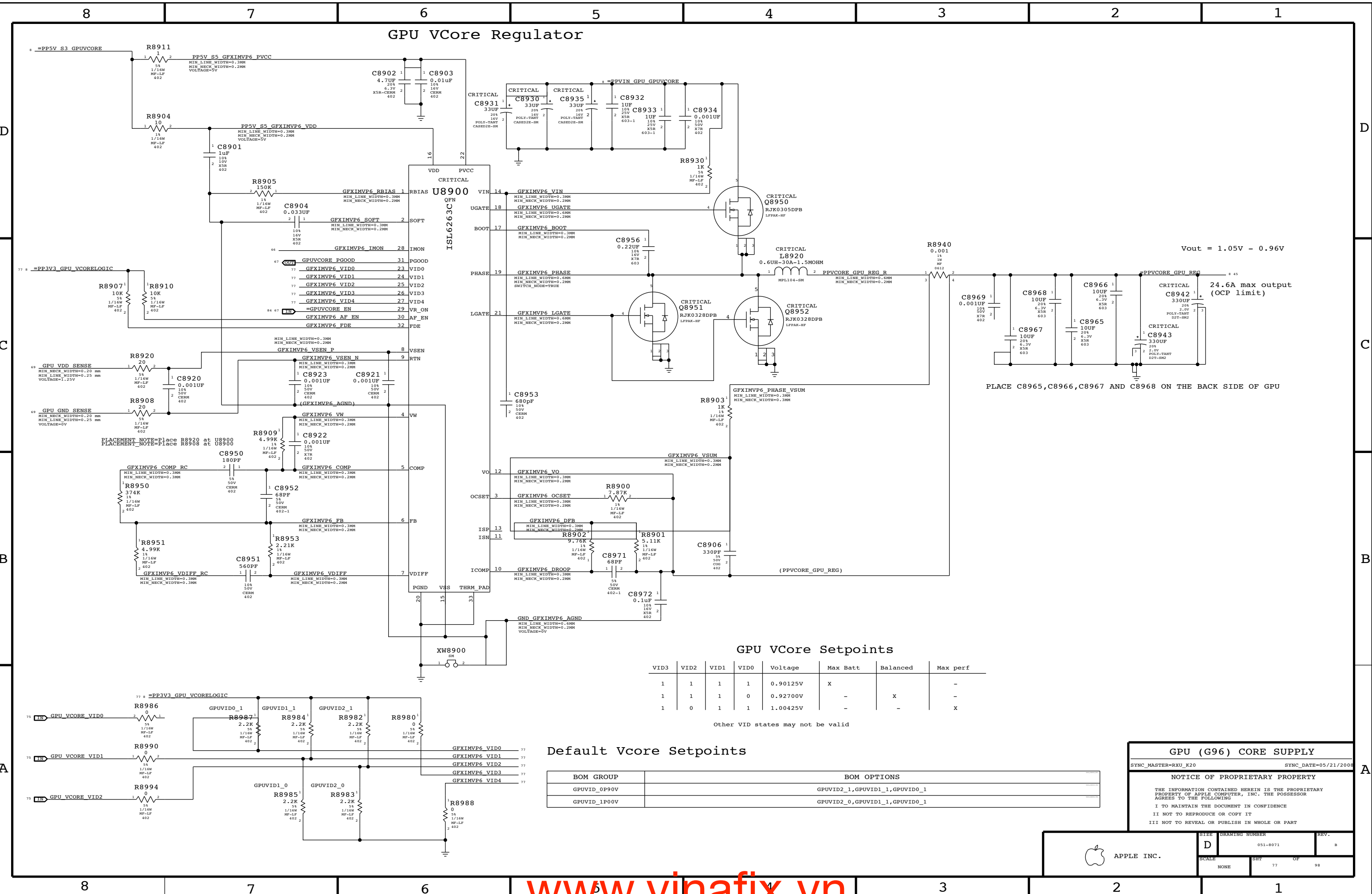
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SIZE D	DRAWING NUMBER 051-8071	REV. B
SCALE NONE	SHT 74	OF 98



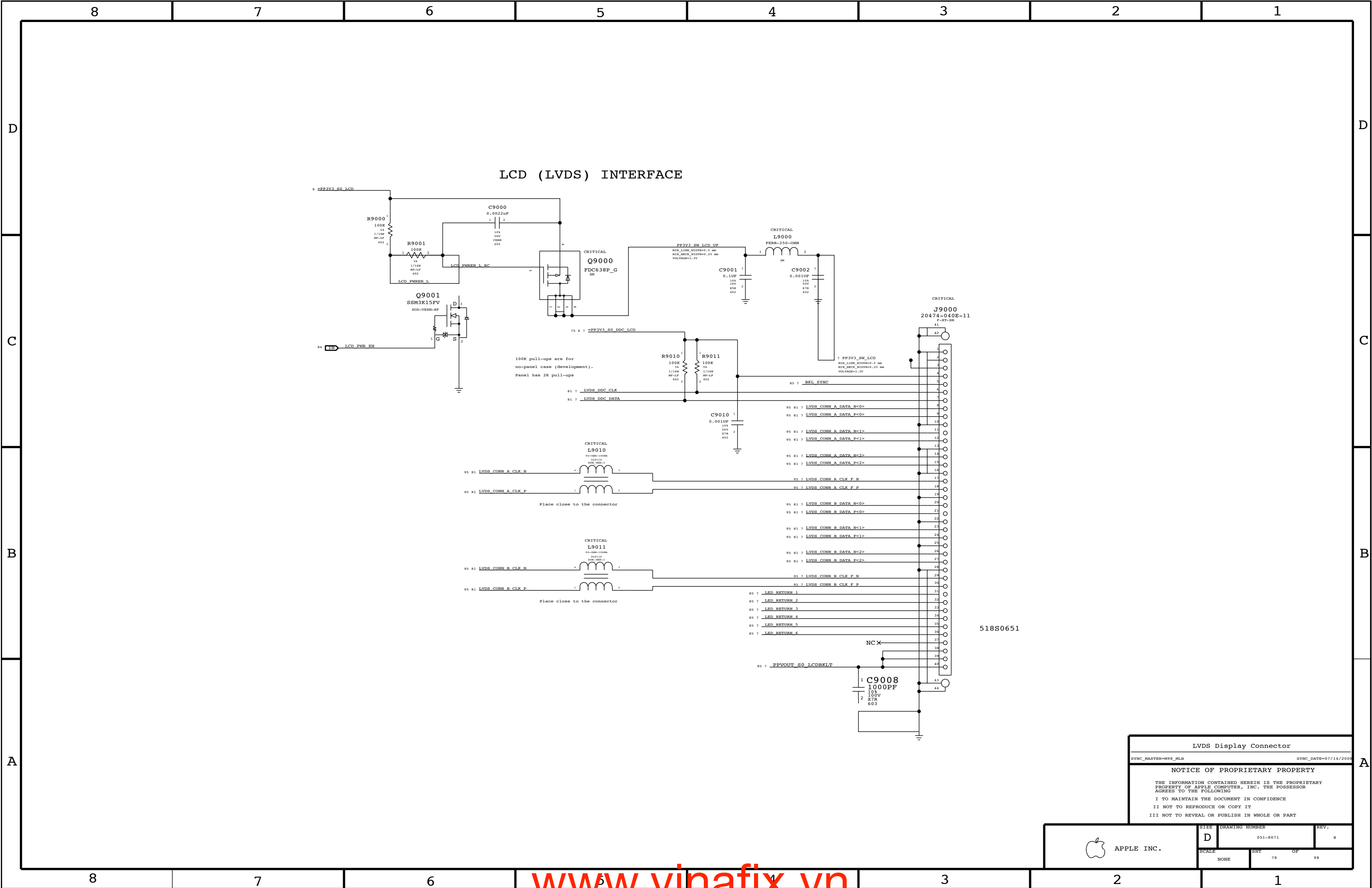


Other VID states may not be valid

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

SIZE D	DRAWING NUMBER 051-8071	REV. B
SCALE NONE	SHT 77	OF 98





LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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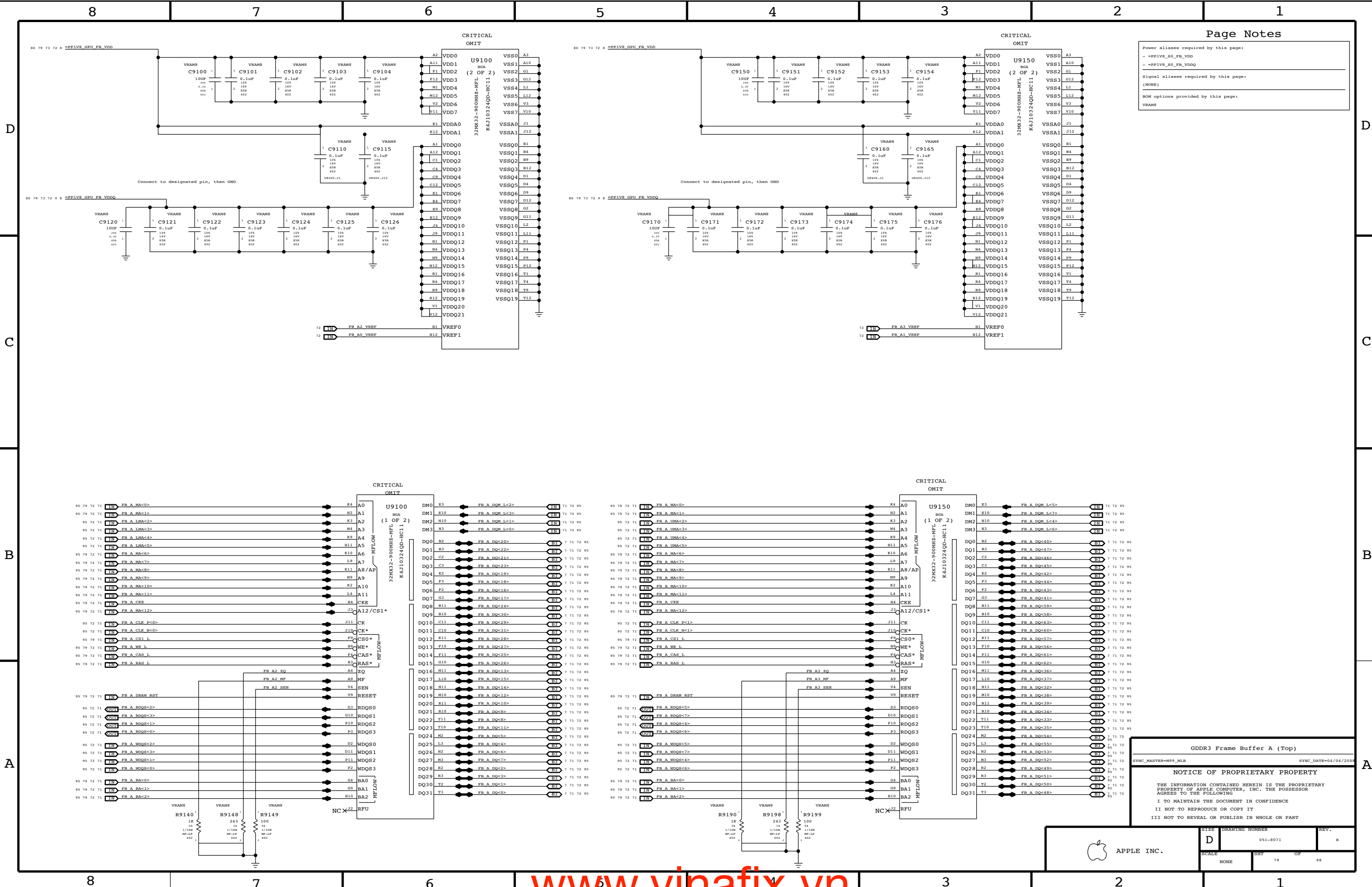
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	D	051-8071	B
SCALE		SBT	OF
NONE		78	98



Page Notes

Power aliases required by this page:

- ~PP1V8_S0_FB_VDD
- ~PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8

GDDR3 Frame Buffer A (Top)

SYNC MASTER=M99_MLB SYNC_DATE=04/04/2008

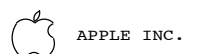
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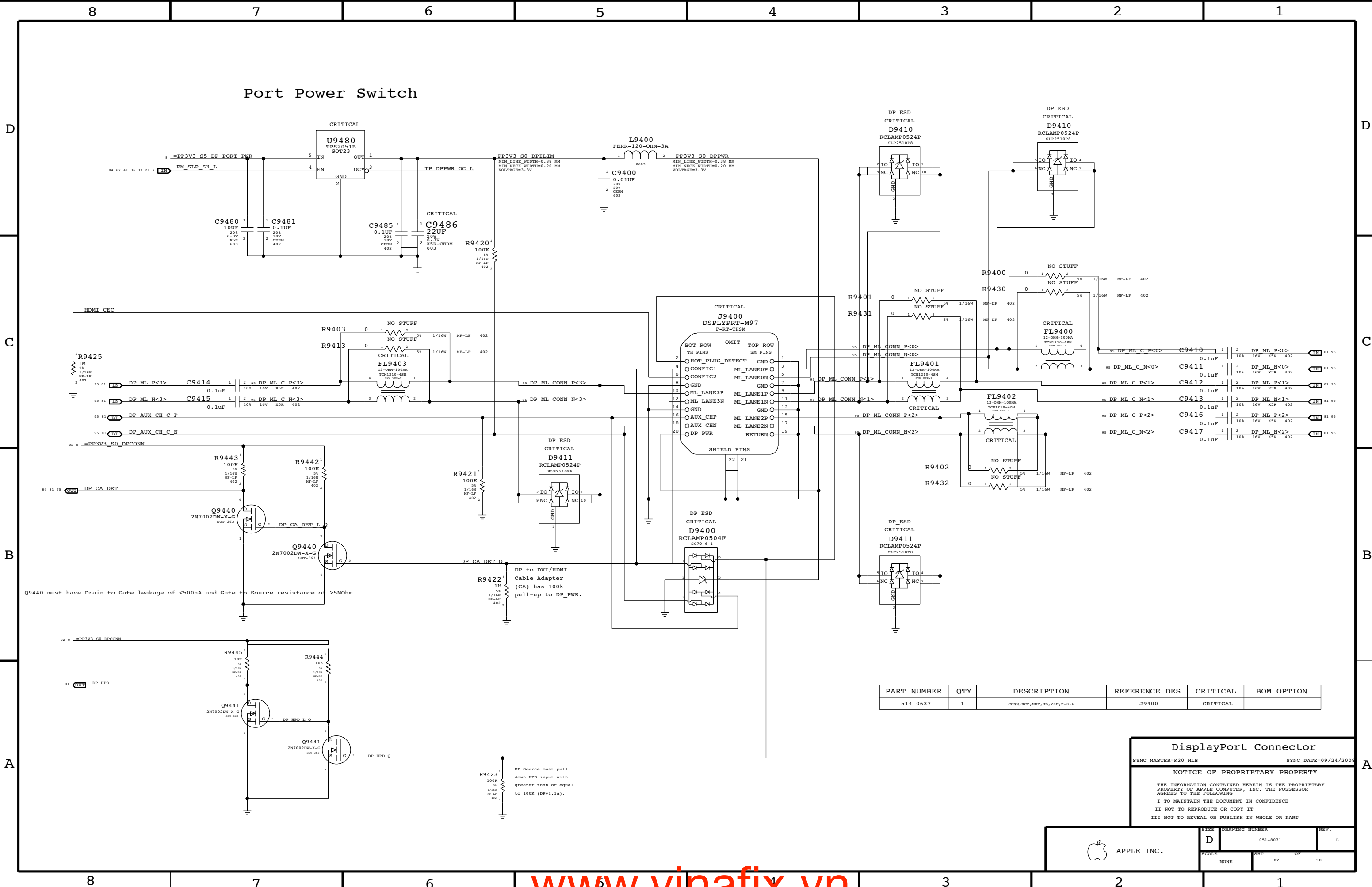
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SIZE	D	DRAWING NUMBER	051-8071	REV.	B
SCALE	NONE	SHEET	79	OF	98







PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN, RCP, MDP, HB, 20P, P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008


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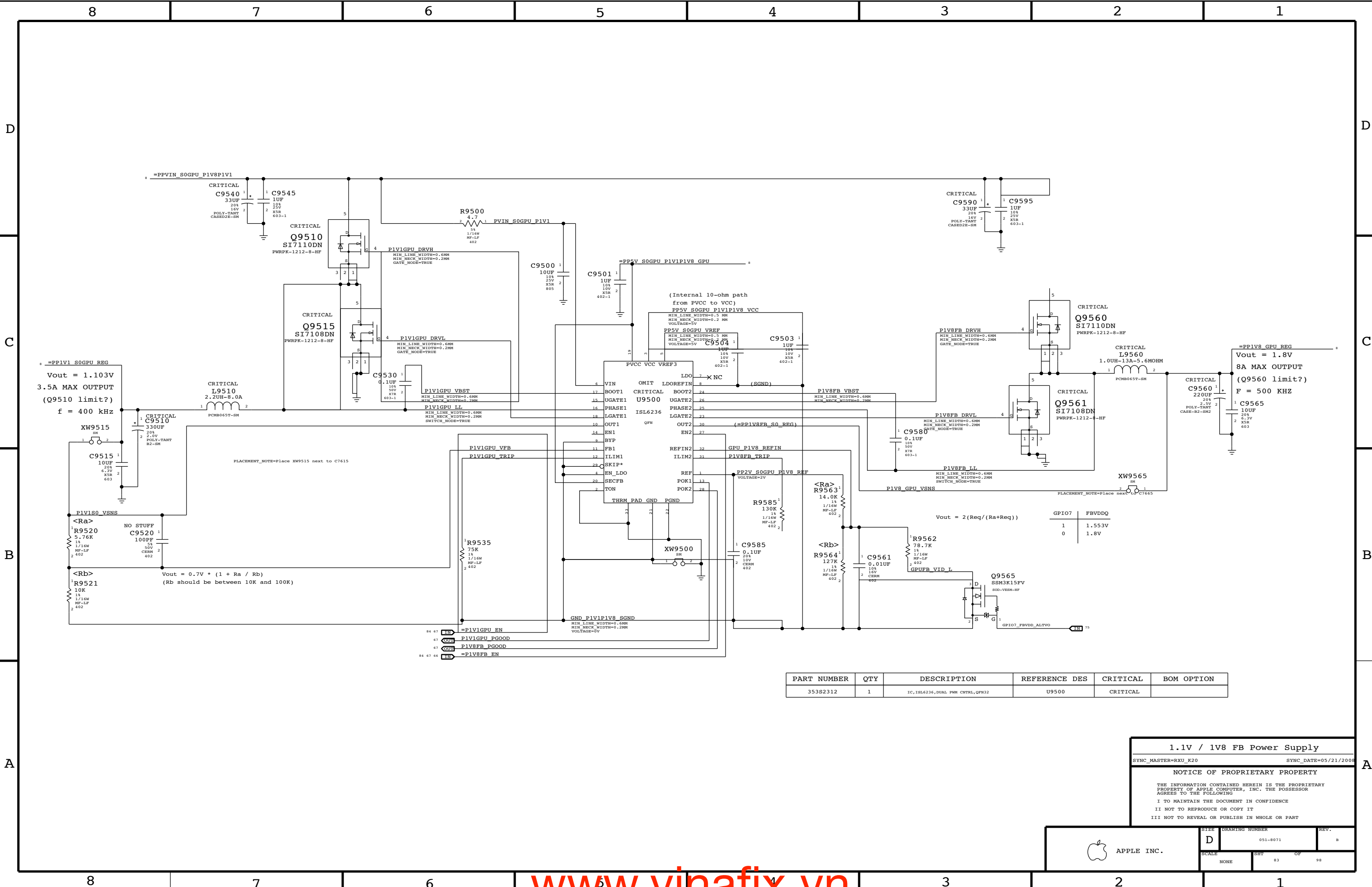
SCALE

NONE

82

OF

98



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
35382312	1	IC, ISL6236, DUAL PWM CTRL, QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008


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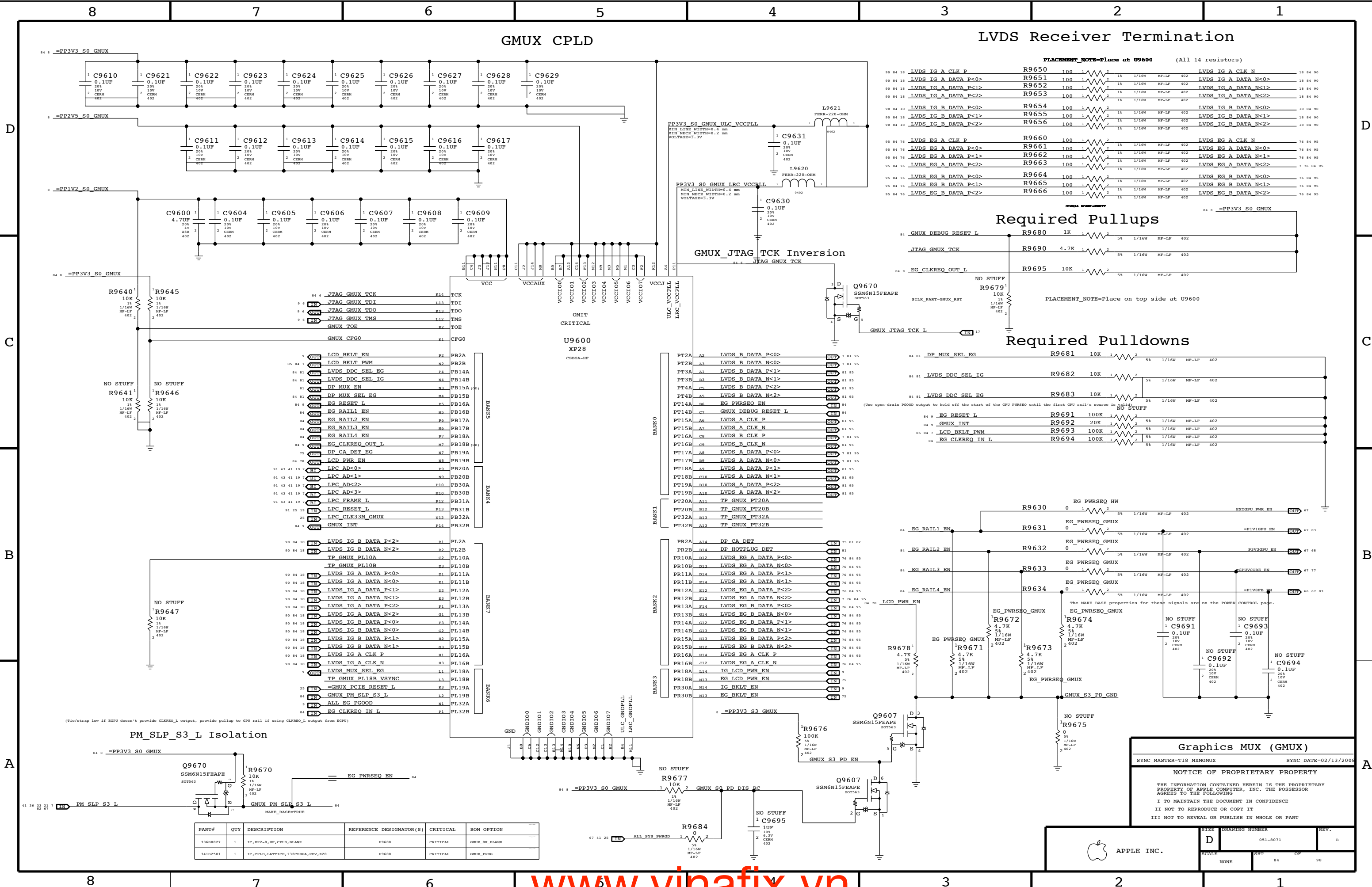
NONE

SBT

83

OF

98



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33680027	1	IC, XP2-8, HF, CPLD, BLANK	U9600	CRITICAL	GMUX_SK_BLANK
34182501	1	IC, CPLD, LATTICE, 132CSBGA, REV, K20	U9600	CRITICAL	GMUX_PROD

Graphics MUX (GMUX)

SYNC_MASTER=T18 MXMGMUX SYNC_DATE=02/13/2008

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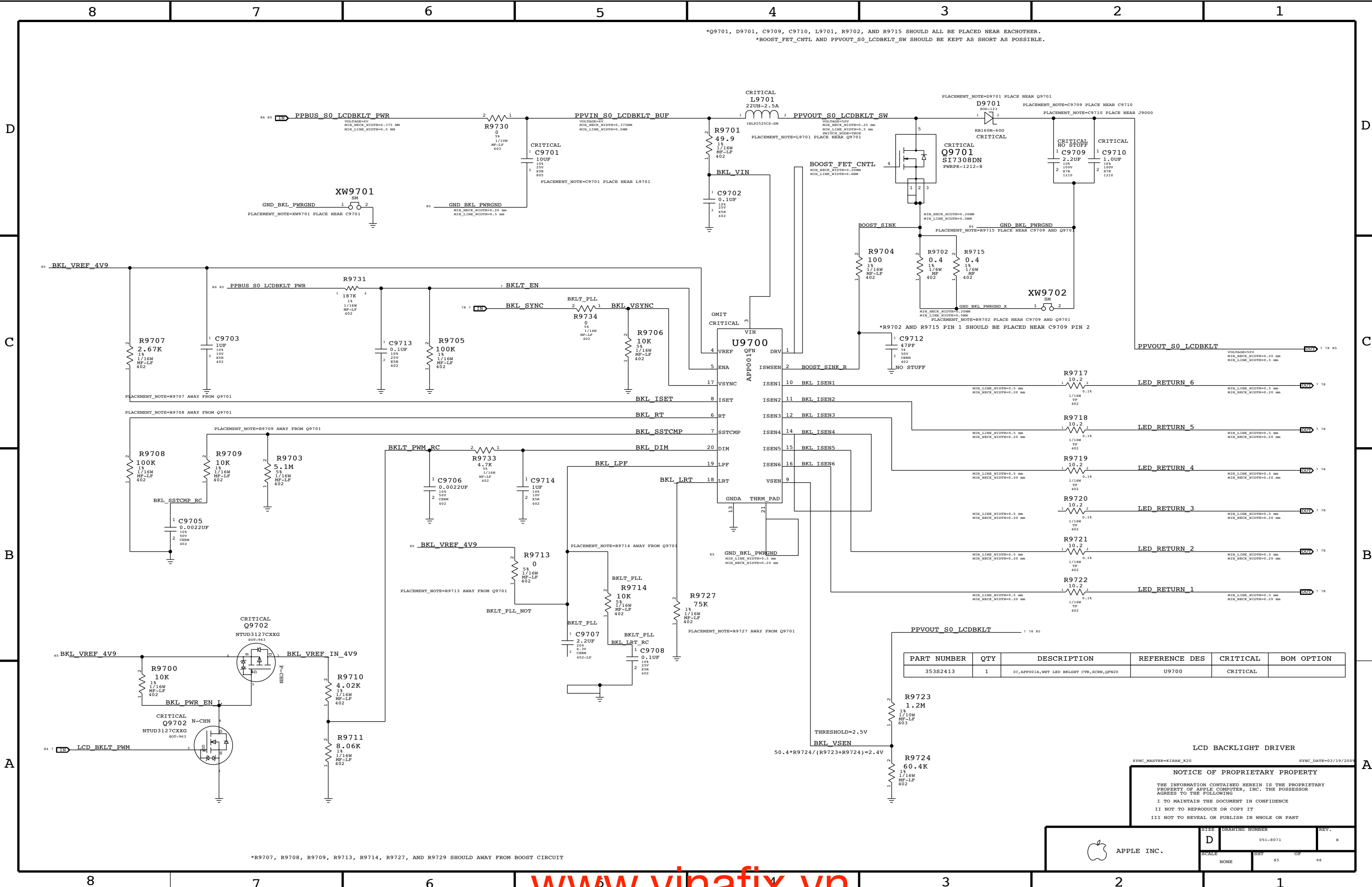
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SCALE SBT 84 OF 98



*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
35382413	1	IC, APP001A, WHF LED BKLGHT CTR, SCRN, QFN20	U9700	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN_K20
SYNC_DATE=03/19/2009

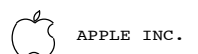
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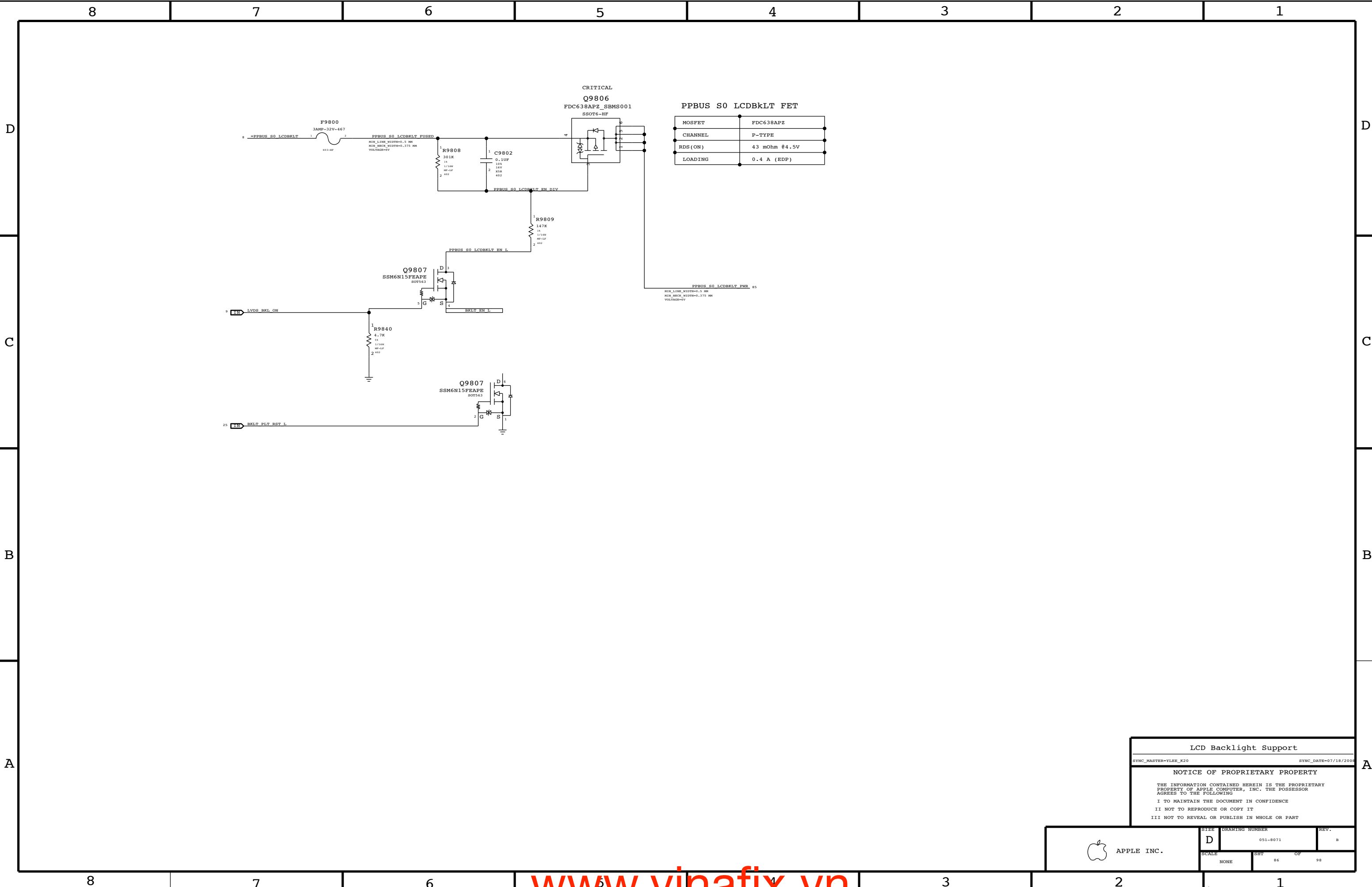
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NONE	85	98



LCD Backlight Support

SYNC_MASTER=VLEE_K20 SYNC_DATE=07/18/2008


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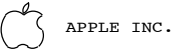
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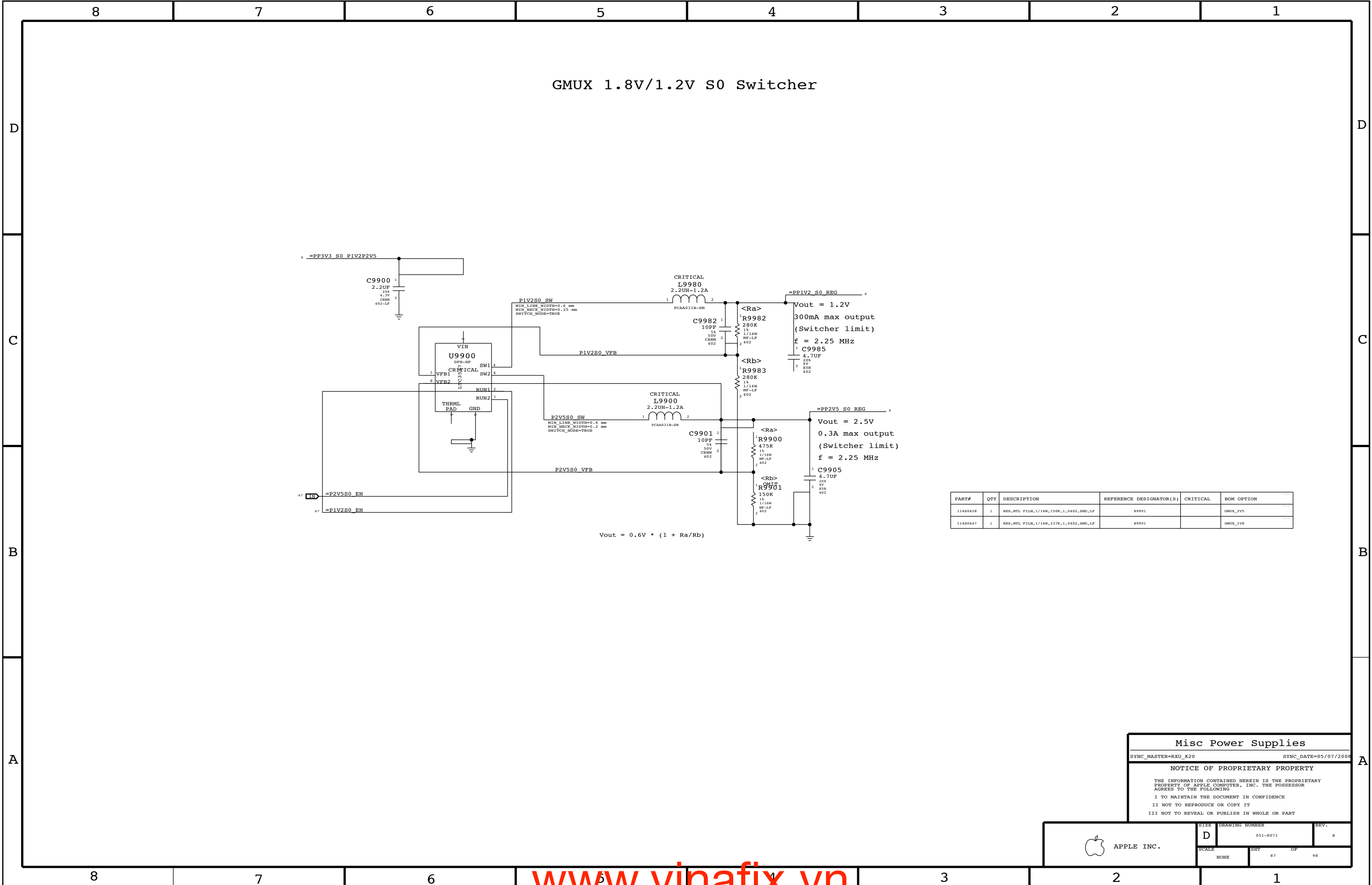
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	SCALE	SHT		OF
	NONE	86		98



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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15	27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15	27
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15	27
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	15	27
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15	27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15	27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15	27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L	15	27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L	15	27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L	15	27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15	27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15	27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15	27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15	27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15	27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15	27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15	27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15	27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15	27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15	27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15	27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15	27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15	27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15	27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15	27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15	27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15	27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15	27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15	27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15	27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15	27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15	27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15	27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15	27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15	27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15	27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15	27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15	27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15	27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15	27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15	27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15	27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15	28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15	28
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15	28
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	15	28
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15	28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15	28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15	28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L	15	28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L	15	28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L	15	28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15	28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15	28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15	28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15	28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15	28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15	28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15	28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15	28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15	28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15	28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15	28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15	28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15	28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15	28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15	28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15	28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15	28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15	28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15	28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15	28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15	28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15	28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15	28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15	28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15	28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15	28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15	28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15	28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15	28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15	28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15	28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15	28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16	
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16	

Memory Constraints

SYNC_MASTER=M98_MLB

SYNC_DATE=04/01/2008

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[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x DIELECTRIC	?
LVDS	*	=3x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP, BOTTOM	=4x _{min} DIELECTRIC	?
LVDS	TOP, BOTTOM	=4x _{min} DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001 v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	PCIE_90D	PCIE	PEG R2D P<15..0>	69
	PCIE_90D	PCIE	PEG R2D N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>	9 69
	PCIE_90D	PCIE	PEG R2D C N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>	9 69
	PCIE_90D	PCIE	PEG D2R N<15..0>	9 69
	PCIE_90D	PCIE	PEG D2R C P<15..0>	69
	PCIE_90D	PCIE	PEG D2R C N<15..0>	69
	PCIE_90D	PCIE	PCIE MINI R2D P	7 30
	PCIE_90D	PCIE	PCIE MINI R2D N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE MINI R2D C P	17 30
	PCIE_90D	PCIE	PCIE MINI R2D C N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE MINI D2R P	7 17 30
	PCIE_90D	PCIE	PCIE MINI D2R N	7 17 30
	PCIE_90D	PCIE	PCIE FW R2D P	35
	PCIE_90D	PCIE	PCIE FW R2D N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P	17 35
	PCIE_90D	PCIE	PCIE FW R2D C N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P	17 35
	PCIE_90D	PCIE	PCIE FW D2R N	17 35
	PCIE_90D	PCIE	PCIE FW D2R C P	35
	PCIE_90D	PCIE	PCIE FW D2R C N	35
	PCIE_90D	PCIE	PCIE EXCARD R2D P	7 31
	PCIE_90D	PCIE	PCIE EXCARD R2D N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE EXCARD R2D C P	17 31
	PCIE_90D	PCIE	PCIE EXCARD R2D C N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE EXCARD D2R P	7 17 31
	PCIE_90D	PCIE	PCIE EXCARD D2R N	7 17 31
MCP_PEG_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N	17 69
MCP_PEG1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	17 30
MCP_PEG2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N	17 35
MCP_PEG1_EXREFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX CLK COMP	17
CRT_RED	CRT_50R	CRT	CRT IG R C PR	18 24
CRT_GREEN	CRT_50R	CRT	CRT IG G Y Y	18 24
CRT_BLUE	CRT_50R	CRT	CRT IG B COMP PB	18 24
CRT_SYNC	CRT_50R	CRT_SYNC	CRT IG HSYNC	18 24
CRT_SYNC	CRT_50R	CRT_SYNC	CRT IG VSYNC	18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET	18 24
MCP_DAC_VREF		MCP_TV_DAC_COMP	MCP TV DAC VREF	18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS IG TXC P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS IG TXC N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP IG ML P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP IG ML N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP HDMI RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP HDMI VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>	18 84
LVDS_IG_A_DATA1	LVDS_100D	LVDS	LVDS IG A DATA P<3>	9 18
LVDS_IG_A_DATA1	LVDS_100D	LVDS	LVDS IG A DATA N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>	18 84
LVDS_IG_B_DATA1	LVDS_100D	LVDS	LVDS IG B DATA P<3>	9 18
LVDS_IG_B_DATA1	LVDS_100D	LVDS	LVDS IG B DATA N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET	18 24
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE	18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA HDD R2D C P	20 38
	SATA_100D	SATA	SATA HDD R2D C N	20 38
	SATA_100D	SATA	SATA HDD R2D P	7 38
	SATA_100D	SATA	SATA HDD R2D N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA HDD D2R P	20 38
	SATA_100D	SATA	SATA HDD D2R N	20 38
	SATA_100D	SATA	SATA HDD D2R C P	7 38
	SATA_100D	SATA	SATA HDD D2R C N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D C P	20 38
	SATA_100D	SATA	SATA ODD R2D C N	20 38
	SATA_100D	SATA	SATA ODD R2D P	7 38
	SATA_100D	SATA	SATA ODD R2D N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R P	20 38
	SATA_100D	SATA	SATA ODD D2R N	20 38
	SATA_100D	SATA	SATA ODD D2R C P	7 38
	SATA_100D	SATA	SATA ODD D2R C N	7 38
MCP_SATA_TERM		SATA_TERM	MCP SATA TERM	20

MCP Constraints 1	
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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?






















SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 18
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 18
	MCP_CLK25M_BUF0	ENET_MII_558	MCP_BUF0_CLK	MCP CLK25M BUF0 R 18 33
		ENET_MII_558	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1 32 33
	ENET_INTR_I	ENET_MII_558	ENET_MII	ENET INTR L
	ENET_MDIO	ENET_MII_558	ENET_MII	ENET MDIO 18 32
	ENET_MDC	ENET_MII_558	ENET_MII	ENET MDC 18 32
	ENET_PWDOWN_I	ENET_MII_558	ENET_MII	ENET PWRDWN L
		ENET_MII_558	ENET_MII	ENET CLK125M RXCLK R 32
	ENET_RXCLK	ENET_MII_558	ENET_MII	ENET CLK125M RXCLK 18 32
		ENET_MII_558	ENET_MII	ENET RXD R<3..0> 18 32
	ENET_RXD	ENET_MII_558	ENET_MII	ENET RXD<0> 32
	ENET_RXD_CSTRAP	ENET_MII_558	ENET_MII	ENET RXD<3..1> 18 32
	ENET_RXD	ENET_MII_558	ENET_MII	ENET RX CTRL 18 32
		ENET_MII_558	ENET_MII	ENET CLK125M TXCLK 18 32
	ENET_TXD0	ENET_MII_558	ENET_MII	ENET TXD<0> 18 32
	ENET_TXD	ENET_MII_558	ENET_MII	ENET TXD<3..1> 18 32
	ENET_TXD	ENET_MII_558	ENET_MII	ENET TX CTRL 18 32
		ENET_MII_558	ENET_MII	ENET RESET L 18 32
	ENET_MDY	ENET_MII_100D	ENET_MDY	ENET MDI P<3..0> 32 34
		ENET_MDY_100D	ENET_MDY	ENET MDI N<3..0> 32 34

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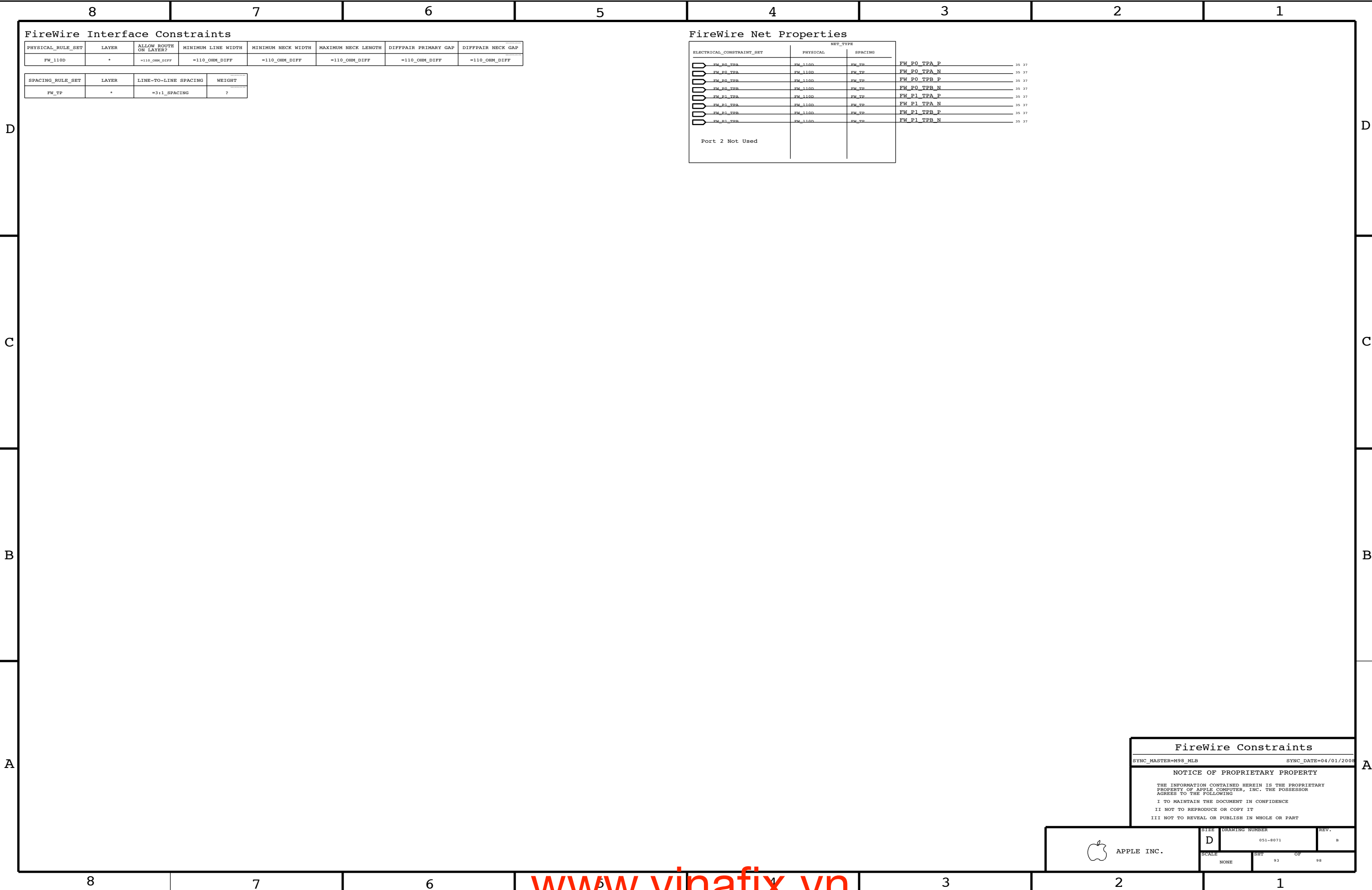


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D	051-8071	B
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FireWire Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties			
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P 35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N 35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P 35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N 35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P 35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N 35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P 35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N 35 37
Port 2 Not Used			

FireWire Constraints

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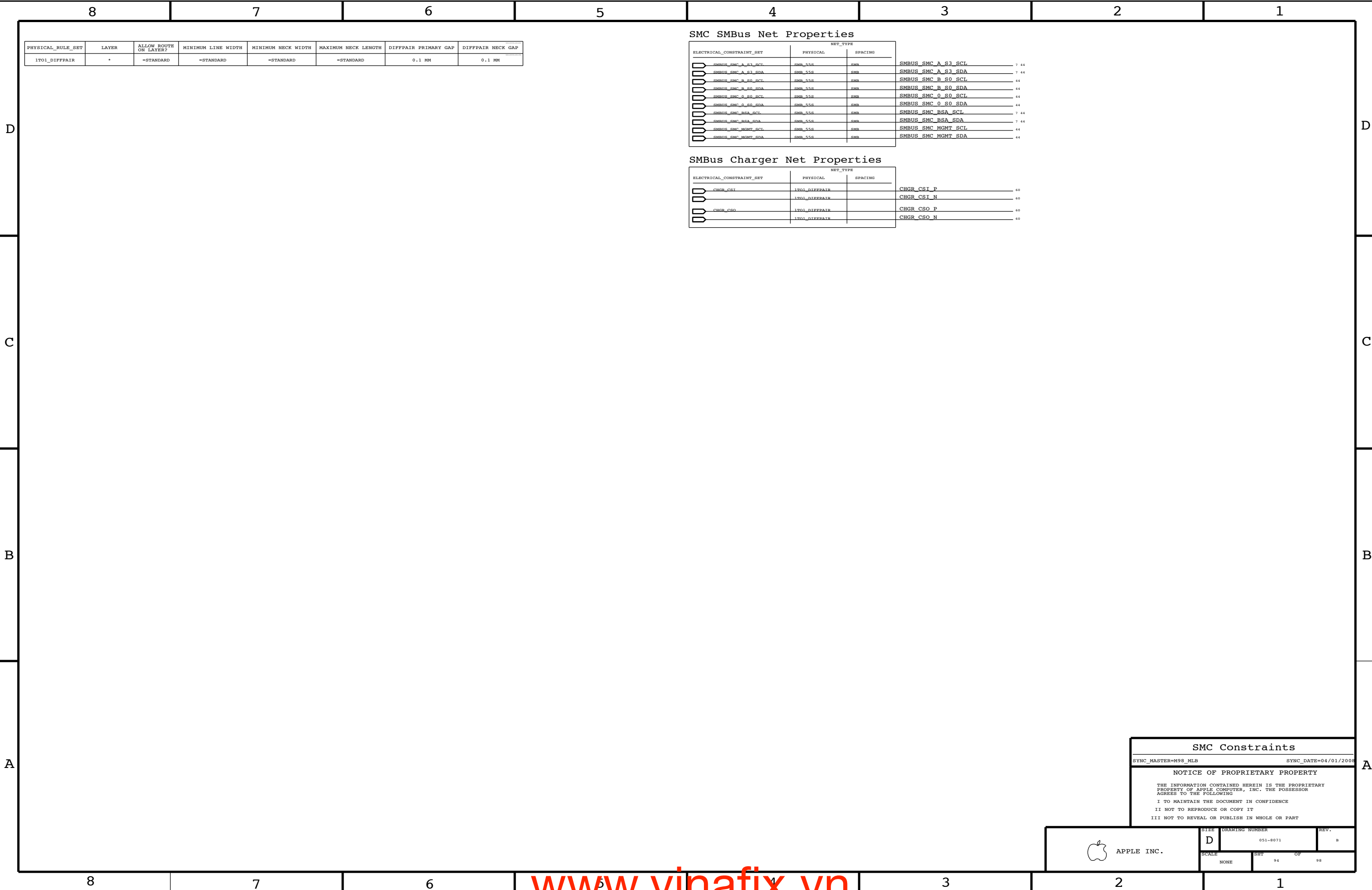
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NONE	93	98



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40WS5E	*	=+0_OHM_SE	=+0_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=+0_OHM_SE	=+0_OHM_SE	0.095 MM	=+0_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=+0_OHM_DIFF	=+0_OHM_DIFF	0.095 MM	=+0_OHM_DIFF	=+0_OHM_DIFF	=+0_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GD0R3_CLK	*	=2.5+1_SPACING	?
GD0R3_CMD	*	=2.5+1_SPACING	?
GD0R3_DATA	*	=2.5+1_SPACING	?
GD0R3_DQS	*	=2.5+1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCF79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.















MUXGFX Net Properties

ELECTRICAL_CONSTRAINTSET		REF_TYPE		
		PHYSICAL	SPACING	
U118	LVDS_A_CLK	LVDS_1000	LVDS	LVDS_A_CLK P 81 84
U119	LVDS_A_CLK	LVDS_1000	LVDS	LVDS_A_CLK N 81 84
U200	LVDS_B_DATA	LVDS_1000	LVDS	LVDS_B_DATA P<2..0> 7 81 84
U201	LVDS_B_DATA	LVDS_1000	LVDS	LVDS_B_DATA N<2..0> 7 81 84
U202	LVDS_B_CLK	LVDS_1000	LVDS	LVDS_B_CLK P 7 81 84
U203	LVDS_B_CLK	LVDS_1000	LVDS	LVDS_B_CLK N 81 84
U204	LVDS_B_DATA	LVDS_1000	LVDS	LVDS_B_DATA P<2..0> 7 81 84
U205	LVDS_B_DATA	LVDS_1000	LVDS	LVDS_B_DATA N<2..0> 7 81 84
U206		LVDS_1000	LVDS	LVDS_CONN A_CLK F P 7 78
U207		LVDS_1000	LVDS	LVDS_CONN A_CLK F N 7 78
U208		LVDS_1000	LVDS	LVDS_CONN B_CLK F P 7 78
U209		LVDS_1000	LVDS	LVDS_CONN B_CLK F N 7 78
U210		LVDS_1000	LVDS	LVDS_CONN A_CLK P 78 81
U211		LVDS_1000	LVDS	LVDS_CONN A_CLK N 78 81
U212		LVDS_1000	LVDS	LVDS_CONN A_DATA P<2..0> 7 78 81
U213		LVDS_1000	LVDS	LVDS_CONN A_DATA N<2..0> 7 78 81
U214		LVDS_1000	LVDS	LVDS_CONN B_CLK P 78 81
U215		LVDS_1000	LVDS	LVDS_CONN B_CLK N 78 81
U216		LVDS_1000	LVDS	LVDS_CONN B_DATA P<2..0> 7 78 81
U217		LVDS_1000	LVDS	LVDS_CONN B_DATA N<2..0> 7 78 81
U218				
U219	DP_ML	DP_1000	DISPLAYPORT	DP ML, C P<3..0> 82
U220		DP_1000	DISPLAYPORT	DP ML, C N<3..0> 82
U221	DP_ML	DP_1000	DISPLAYPORT	DP ML P<3..0> 81 82
U222		DP_1000	DISPLAYPORT	DP ML N<3..0> 81 82
U223	DP_ML	DP_1000	DISPLAYPORT	DP ML_CONN P<3..0> 82
U224		DP_1000	DISPLAYPORT	DP ML_CONN N<3..0> 82
U225	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH C P 81 82
U226	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH C N 81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINTSET		NET_TYPE			
		PHYSICAL	SPACING		
	FB_A_CLE_P<0>	00001_800	00001_CLE	FB A CLE P<0>	71 72 79
		00001_800	00001_CLE	FB A CLE N<0>	71 72 79
	FB_B_CLE_P	00001_800	00001_CLE	FB A CLE P<1>	71 72 79
		00001_800	00001_CLE	FB A CLE N<1>	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A MAC1..0>	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A MAC12..6>	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A BAC2..0>	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A RAS L	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A CAS L	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A WE L	71 72 79
	FB_AB_C00_E0	00001_400500	00001_C00	FB A CKE	71 72 79
	FB_AB_C00	00001_400500	00001_C00	FB A C00 L	71 72
	FB_AB_C00_E0	00001_400500	00001_C00	FB A DRAM RST	71 72 79
	FB_A_C00	00001_4000	00001_C00	FB A LMA<5..2>	71 72 79
	FB_B_C00	00001_4000	00001_C00	FB A UMA<5..2>	71 72 79
	FB_A_WD000	00001_4000	00001_W00	FB A WD00<0>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A WD00<1>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A WD00<2>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A WD00<3>	71 72 79
	FB_A_WD000	00001_4000	00001_W00	FB A RD00<0>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A RD00<1>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A RD00<2>	71 72 79
	FB_A_WD001	00001_4000	00001_W00	FB A RD00<3>	71 72 79
	FB_A_DQ_0000	00001_4000	00001_DATA	FB A DQ<7..0>	7 71 72 79
	FB_A_DQ_0001	00001_4000	00001_DATA	FB A DQ<15..8>	7 71 72 79
	FB_A_DQ_0002	00001_4000	00001_DATA	FB A DQ<23..16>	7 71 72 79
	FB_A_DQ_0003	00001_4000	00001_DATA	FB A DQ<31..24>	7 71 72 79
	FB_B_D000	00001_4000	00001_DATA	FB A DQM L<0>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<1>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<2>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<3>	71 72 79
	FB_B_WD000	00001_4000	00001_W00	FB A WD00<4>	71 72 79
	FB_B_WD001	00001_4000	00001_W00	FB A WD00<5>	71 72 79
	FB_B_WD001	00001_4000	00001_W00	FB A WD00<6>	71 72 79
	FB_B_WD001	00001_4000	00001_W00	FB A WD00<7>	71 72 79
	FB_B_RD000	00001_4000	00001_W00	FB A RD00<4>	71 72 79
	FB_B_RD001	00001_4000	00001_W00	FB A RD00<5>	71 72 79
	FB_B_RD001	00001_4000	00001_W00	FB A RD00<6>	71 72 79
	FB_B_RD001	00001_4000	00001_W00	FB A RD00<7>	71 72 79
	FB_B_DQ_0000	00001_4000	00001_DATA	FB A DQ<39..32>	7 71 72 79
	FB_B_DQ_0001	00001_4000	00001_DATA	FB A DQ<47..40>	7 71 72 79
	FB_B_DQ_0002	00001_4000	00001_DATA	FB A DQ<55..48>	7 71 72 79
	FB_B_DQ_0003	00001_4000	00001_DATA	FB A DQ<63..56>	7 71 72 79
	FB_B_D000	00001_4000	00001_DATA	FB A DQM L<4>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<5>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<6>	71 72 79
	FB_B_D001	00001_4000	00001_DATA	FB A DQM L<7>	71 72 79
1270	FB_AB_C01	00001_400500	00001_C00	FB A C01 L	71 79

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET		RET_TYPE		
		PHYSICAL	SPACING	
	CK330_P02361	CLK_STOP_3V3	CLK_STOP	GPU_CLK27M 75
	CK330_CLK27M04	CLK_STOP_3V3	CLK_STOP	GPU_CLK27M_SS 75
	LVDS_EG_A_CLK	LVDS_1000	LVDS	LVDS_EG_A_CLK_P 76 84
	LVDS_EG_A_CLK	LVDS_1000	LVDS	LVDS_EG_A_CLK_N 76 84
	LVDS_EG_A_DATA	LVDS_1000	LVDS	LVDS_EG_A_DATA_P<2..0> 76 84
	LVDS_EG_A_DATA	LVDS_1000	LVDS	LVDS_EG_A_DATA_N<2..0> 7 76 84
	LVDS_EG_B_DATA	LVDS_1000	LVDS	LVDS_EG_B_DATA_P<2..0> 76 84
	LVDS_EG_B_DATA	LVDS_1000	LVDS	LVDS_EG_B_DATA_N<2..0> 76 84
	DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0> 76
	DP_MT	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0> 76
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P 76
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N 76
	DP	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P 81
	DP	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N 81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
FB_C_CLK_P<0>	00001_800	00001_CLK	FB B CLK_P<0>	71 73 80
FB_B_CLK_P<0>	00001_800	00001_CLK	FB B CLK_N<0>	71 73 80
FB_B_CLK_P<1>	00001_800	00001_CLK	FB B CLK_P<1>	71 73 80
FB_B_CLK_N<1>	00001_800	00001_CLK	FB B CLK_N<1>	71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B MAC<1..0>	71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B MAC<12..6>	7 71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B BAS<2..0>	7 71 73
FB_C0_C00	00001_000100	00001_C00	FB B BAS_L	71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B CAS_L	7 71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B WE_L	71 73 80
FB_C0_C00_00	00001_000100	00001_C00	FB B CKE	71 73 80
FB_C0_C00	00001_000100	00001_C00	FB B C00_L	7 71 73
FB_C0_C00_00	00001_000100	00001_C00	FB B DRAM_RST	71 73 80
FB_C_C00	00001_0000	00001_C00	FB B LMA<5..2>	71 73 80
FB_B_C00	00001_0000	00001_C00	FB B UMA<5..2>	71 73 80
FB_C_WDQ00	00001_0000	00001_P00	FB B WDQ0<0>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B WDQ0<1>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B WDQ0<2>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B WDQ0<3>	71 73 80
FB_C_WDQ00	00001_0000	00001_P00	FB B RDQ0<0>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B RDQ0<1>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B RDQ0<2>	71 73 80
FB_C_WDQ01	00001_0000	00001_P00	FB B RDQ0<3>	71 73 80
FB_C_DQ_00_0000	00001_0000	00001_DATA	FB B DQ<7..0>	7 71 73 80
FB_C_DQ_00_0001	00001_0000	00001_DATA	FB B DQ<15..8>	7 71 73 80
FB_C_DQ_00_0002	00001_0000	00001_DATA	FB B DQ<23..16>	7 71 73 80
FB_C_DQ_00_0003	00001_0000	00001_DATA	FB B DQ<31..24>	7 71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<0>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<1>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<2>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<3>	71 73 80
FB_B_WDQ00	00001_0000	00001_P00	FB B WDQ0<4>	71 73 80
FB_B_WDQ01	00001_0000	00001_P00	FB B WDQ0<5>	71 73 80
FB_B_WDQ01	00001_0000	00001_P00	FB B WDQ0<6>	71 73 80
FB_B_WDQ01	00001_0000	00001_P00	FB B WDQ0<7>	71 73 80
FB_B_RDQ00	00001_0000	00001_P00	FB B RDQ0<4>	71 73 80
FB_B_RDQ01	00001_0000	00001_P00	FB B RDQ0<5>	71 73 80
FB_B_RDQ01	00001_0000	00001_P00	FB B RDQ0<6>	71 73 80
FB_B_RDQ01	00001_0000	00001_P00	FB B RDQ0<7>	71 73 80
FB_B_DQ_00_0000	00001_0000	00001_DATA	FB B DQ<39..32>	7 71 73 80
FB_B_DQ_00_0001	00001_0000	00001_DATA	FB B DQ<47..40>	7 71 73 80
FB_B_DQ_00_0002	00001_0000	00001_DATA	FB B DQ<55..48>	7 71 73 80
FB_B_DQ_00_0003	00001_0000	00001_DATA	FB B DQ<63..56>	7 71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<4>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<5>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<6>	71 73 80
FB_B_DQM0	00001_0000	00001_DATA	FB B DQM_L<7>	71 73 80
FB_C0_C01	00001_000100	00001_C00	FB B C01_L	71 80

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_558	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I701_558	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2*1_SPACING	?
THERM	*	=2*1_SPACING	?
AUDIO	*	=2*1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1VS_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	GND	*	GND_P20H
MEM_CHD	GND	*	GND_P20H
MEM_CTL	GND	*	GND_P20H
MEM_DATA	GND	*	GND_P20H
MEM_DQS	GND	*	GND_P20H

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2304
CPU_COMP	GND	*	GND_P2304
CPU_CTLREF	GND	*	GND_P2304
CPU_VCCSENSE	GND	*	GND_P2304
FSB_DSTA	FSB_DSTA	*	GND_P2304

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLX_PCIE	GND	*	GND_P2304 <small>net:net-spacing:net-spacing</small>
PCIE	GND	*	GND_P2304 <small>net:net-spacing:net-spacing</small>
SATA	GND	*	GND_P2304 <small>net:net-spacing:net-spacing</small>
USB	GND	*	GND_P2304 <small>net:net-spacing:net-spacing</small>
CLX_PCIE	SR_POWER	*	PNR_P2305 <small>net:net-spacing:net-spacing</small>
SATA	SR_POWER	*	PNR_P2304 <small>net:net-spacing:net-spacing</small>
USB	SR_POWER	*	PNR_P2304 <small>net:net-spacing:net-spacing</small>

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	ISL4, ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD_OVERRIDE	ISL3, ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_OVERRIDE	ISL4, ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD_OVERRIDE	ISL3, ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island. Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL CONSTRAINT SET		REF. TYPE		
		PHYSICAL	SPACING	
		ENET_CONN_P<3..0>	ENETCONN	ENETCONN P<3..0>
		ENET_CONN_N<3..0>	ENETCONN	ENETCONN N<3..0>
		SATA_100D	SATA	SATA_ODD_R2D_UF_P
		SATA_100D	SATA	SATA_ODD_R2D_UF_N
		SATA_100D	SATA	SATA_ODD_D2R_UF_P
		SATA_100D	SATA	SATA_ODD_D2R_UF_N
		SATA_100D	SATA	SATA_HDD_D2R_UF_P
		SATA_100D	SATA	SATA_HDD_D2R_UF_N
		SATA_100D	SATA	SATA_HDD_R2D_UF_P
		SATA_100D	SATA	SATA_HDD_R2D_UF_N
		MCPCOREISNS_P	MCPCOREISNS	MCPCOREISNS_P
		MCPCOREISNS_N	MCPCOREISNS	MCPCOREISNS_N
		CPUTHMENS_D2_P	CPUTHMENS	CPUTHMENS_D2_P
		CPUTHMENS_D2_N	CPUTHMENS	CPUTHMENS_D2_N
		CPU_THERMD_P	CPU_THERMD	CPU_THERMD_P
		CPU_THERMD_N	CPU_THERMD	CPU_THERMD_N
		GPUTHMENS_D_P	GPUTHMENS	GPUTHMENS_D_P
		GPUTHMENS_D_N	GPUTHMENS	GPUTHMENS_D_N
		GPU_TDIODE_P	GPU_TDIODE	GPU_TDIODE_P
		GPU_TDIODE_N	GPU_TDIODE	GPU_TDIODE_N
		MCPTHMENS_D_P	MCPTHMENS	MCPTHMENS_D_P
		MCPTHMENS_D_N	MCPTHMENS	MCPTHMENS_D_N
		MCP_THMDIODE_P	MCP_THMDIODE	MCP_THMDIODE_P
		MCP_THMDIODE_N	MCP_THMDIODE	MCP_THMDIODE_N
		1V05CPUISNS_R_P	1V05CPUISNS	1V05CPUISNS_R_P
		1V05CPUISNS_R_N	1V05CPUISNS	1V05CPUISNS_R_N
		DDRISNS_R_P	DDRISNS	DDRISNS_R_P
		DDRISNS_R_N	DDRISNS	DDRISNS_R_N
		GPUISNS_P	GPUISNS	GPUISNS_P
		GPUISNS_N	GPUISNS	GPUISNS_N
		1V05CPU_P	1V05CPU	1V05CPU_P
		1V05CPU_N	1V05CPU	1V05CPU_N
		DDRISNS_P	DDRISNS	DDRISNS_P
		DDRISNS_N	DDRISNS	DDRISNS_N
		PIV8GPU_P	PIV8GPU	PIV8GPU_P
		PIV8GPU_N	PIV8GPU	PIV8GPU_N
		ISNS_CPU_P	ISNS_CPU	ISNS_CPU_P
		ISNS_CPU_N	ISNS_CPU	ISNS_CPU_N
		GND	GND	GND
		SA_POWER	PP3V3_S5	PP3V3_S5
		SA_POWER	PP3V3_S0	PP3V3_S0
		SA_POWER	PP1V5_S0	PP1V5_S0
		PIV8GPUISNS_P	PIV8GPUISNS	PIV8GPUISNS_P
		PIV8GPUISNS_N	PIV8GPUISNS	PIV8GPUISNS_N
		PIV8GPUISNS_R_P	PIV8GPUISNS	PIV8GPUISNS_R_P
		PIV8GPUISNS_R_N	PIV8GPUISNS	PIV8GPUISNS_R_N
		ASIC_CNTRIMEM1	FLASH_558	NF_CLE_R
		ASIC_CNTRIMEM1	FLASH_558	NF_ALE_R
		ASIC_CNTRIMEM1	FLASH_558	NF_CE0_L_R
		ASIC_CNTRIMEM1	FLASH_558	NF_CE1_L_R
		ASIC_CNTRIMEM1	FLASH_558	NF_RE0_L_R
		ASIC_CNTRIMEM1	FLASH_558	NF_WE0_L_R
		ASIC_CNTRIMEM2	FLASH_558	NF_CLE_R
		ASIC_CNTRIMEM2	FLASH_558	NF_ALE_R
		ASIC_CNTRIMEM2	FLASH_558	NF_CE0_L_R
		ASIC_CNTRIMEM2	FLASH_558	NF_CE1_L_R
		ASIC_CNTRIMEM2	FLASH_558	NF_RE0_L_R
		ASIC_CNTRIMEM2	FLASH_558	NF_WE0_L_R
		ASIC_CNTRIMEM3	FLASH_558	NF_CLE
		ASIC_CNTRIMEM3	FLASH_558	NF_ALE
		ASIC_CNTRIMEM3	FLASH_558	NF_CE0_L
		ASIC_CNTRIMEM3	FLASH_558	NF_CE1_L
		ASIC_CNTRIMEM3	FLASH_558	NF_RE0_L
		ASIC_CNTRIMEM3	FLASH_558	NF_WE0_L
		ASIC_CNTRIMEM2	FLASH_558	NF_CLE
		ASIC_CNTRIMEM2	FLASH_558	NF_ALE
		ASIC_CNTRIMEM2	FLASH_558	NF_CE0_L
		ASIC_CNTRIMEM2	FLASH_558	NF_CE1_L
		ASIC_CNTRIMEM2	FLASH_558	NF_RE0_L
		ASIC_CNTRIMEM2	FLASH_558	NF_WE0_L

M99 Specific Net Properties


ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SMT_TYPE			
			SPACER		
R100	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN P	7 30	
R101	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN N	7 30	
R103	LT01_DIFFPAIR		CHGR CSI_R_P	40	
R104	LT01_DIFFPAIR		CHGR CSI_R_N	40	
R105	LT01_DIFFPAIR		CHGR CSO_R_P	45 60	
R106	LT01_DIFFPAIR		CHGR CSO_R_N	45 60	
R195 (USB_EXTX)	USB_S00	USB	USB2 EXTA MIXED P	39	
R196 (USB_EXTX)	USB_S00	USB	USB2 EXTA MIXED N	39	
R197 (USB_EXTX)	USB_S00	USB	USB2 LT1_P	7 39	
R198 (USB_EXTX)	USB_S00	USB	USB2 LT1_N	7 39	
R199 (USB_EXTD)	USB_S00	USB	CONN TPAD USB_P		
R200 (USB_EXTD)	USB_S00	USB	CONN TPAD USB_N		
R201 (USB_CAMERA)	USB_S00	USB	USB CAMERA CONN_P	7 30	
R202 (USB_CAMERA)	USB_S00	USB	USB CAMERA CONN_N	7 30	
R194	USB_S00	USB	CONN USB2_BT_P	7 30	
R193	USB_S00	USB	CONN USB2_BT_N	7 30	
R192	USB_S00	USB	USB LT2_P	7 39	
R191	USB_S00	USB	USB LT2_N	7 39	
R190	USB_S00	USB	USB2 EXCARD CONN_P	7 31	
R189	USB_S00	USB	USB2 EXCARD CONN_N	7 31	
R188	DP_100D	DP100LXDP00T	DP IG_AUX_CH_C_P	81	
R187	DP_100D	DP100LXDP00T	DP IG_AUX_CH_C_N	81	
R186	MCP PE4 REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FC_P	
R185	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FC_N		
R184	PCIE_FC_R2D	PCIE_S00	PCIE	PCIE_FC_R2D_C_P	
R183	PCIE_FC_R2D	PCIE_S00	PCIE	PCIE_FC_R2D_C_N	
R182	PCIE_FC_D2R	PCIE_S00	PCIE	PCIE_FC_D2R_P	
R181	PCIE_FC_D2R	PCIE_S00	PCIE	PCIE_FC_D2R_N	
R180	PCIE_FC_R2D	PCIE_S00	PCIE	PCIE_FC_R2D_P	
R179	PCIE_FC_R2D	PCIE_S00	PCIE	PCIE_FC_R2D_N	
R178	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD CONN_N	7 31	
R177	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD CONN_P	7 31	
R197	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
R196	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57	
R201	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
R200	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57	
R195	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
R202	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57	
R199	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
R203	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57	
R204	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
R205	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57	
R240					
R240	USB_S00	USB	USB_EXTC_P	20 91 98	
R240	USB_S00	USB	USB_EXTC_N	20 91 98	
R239	USB_S00	USB	USB_LT3_P	7 98	
R238	USB_S00	USB	USB_LT3_N	7 98	

U210	USB_050	USB	USB EXT3 P	20 91 98
U200	USB_050	USB	USB EXT3 N	20 91 98
U20P	USB_050	USB	USB LT3 P	7 98
U21P	USB_050	USB	USB LT3 N	7 98

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	SCALE	SHT	OF	
	NONE		96	98

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M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYFF, BGA			MM	19.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
2TP4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
2TP4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL8, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL8, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL8, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL8, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL8, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_F1MM	*	=DEFAULT	?
BGA_F2MM	*	=DEFAULT	?
BGA_F3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_F1MM
MEM_CLK	*	BGA	BGA_F2MM
CLK_FSB	*	BGA	BGA_F3MM
CLK_PCIE	*	BGA	BGA_F2MM
CLK_SLOW	*	BGA	BGA_F2MM
FSB_DTB	FSB_DTB	BGA	BGA_F3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PCB Rule Definitions

SYNC_MASTER=M99_MLB

SYNC_DATE=04/01/2008

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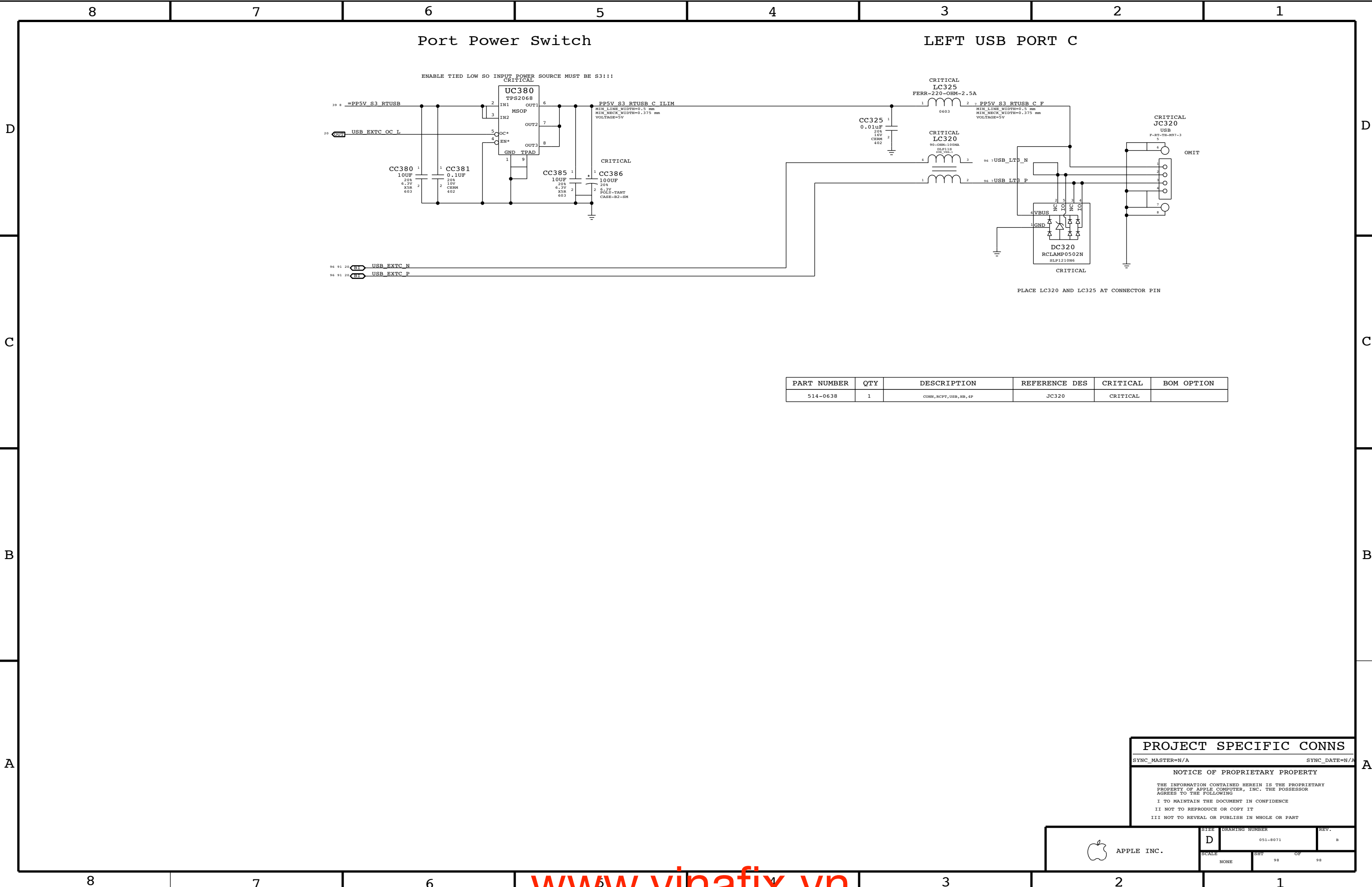
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PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A

SYNC_DATE=N/A


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